# N-Channel Enhancement Mode Field Effect Transistor

## Product Summary

- $V_{DS}$ 40V
- $I_D$ 69A
- $R_{DS(ON)}$( at $V_{GS}$=10V) 5.7mΩ
- 100%

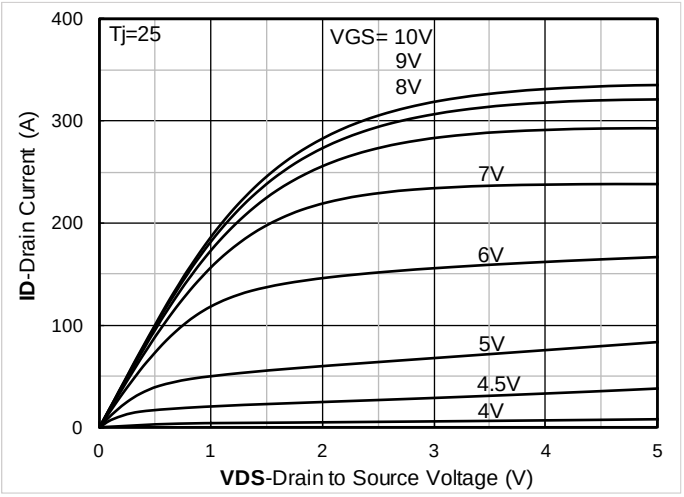



Figure 1. Output Characteristics

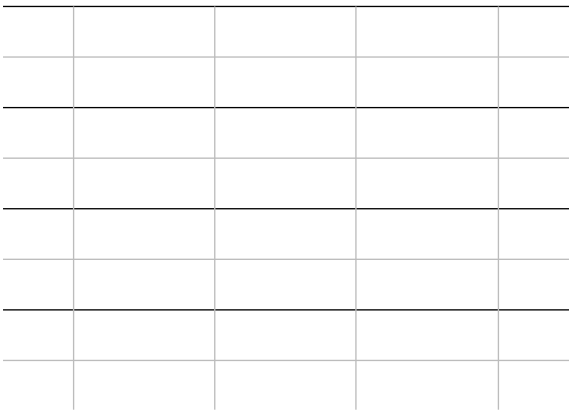


Figure 2. Transfer Characteristics

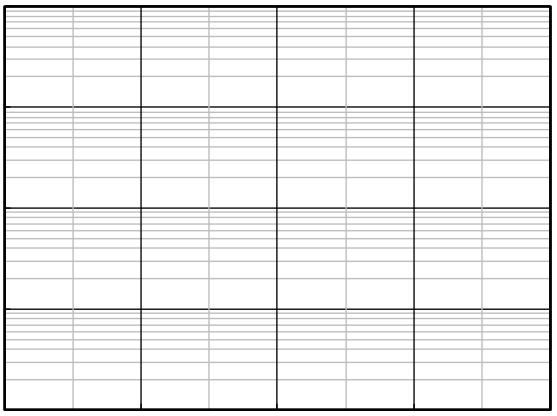


Figure 3. Capacitance Characteristics

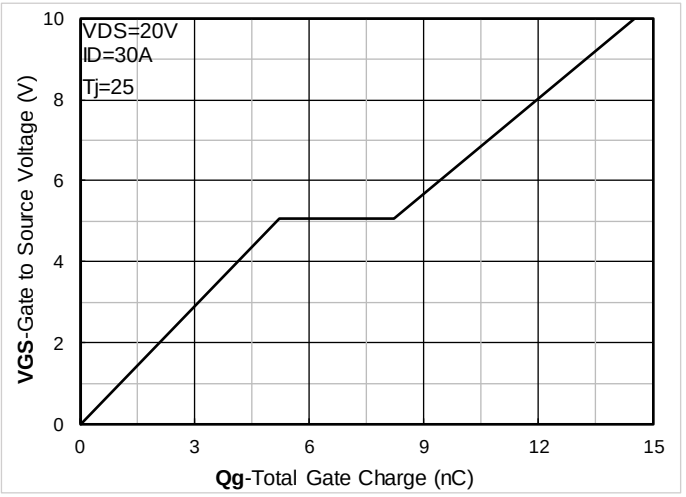



Figure 4. Gate Charge

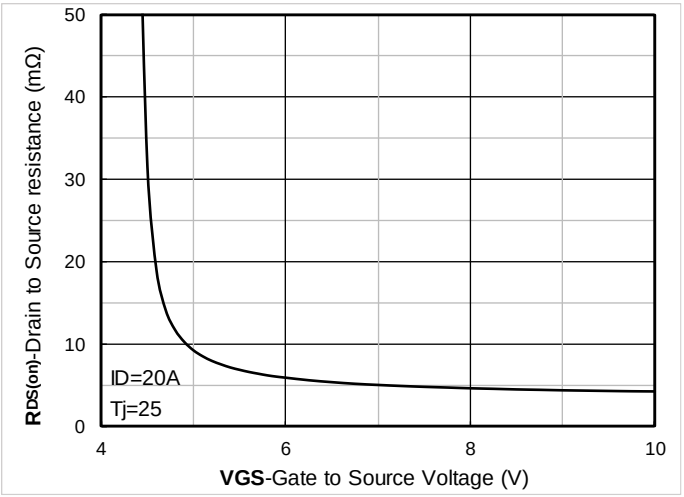



Figure 5. On-Resistance vs Gate to Source Voltage

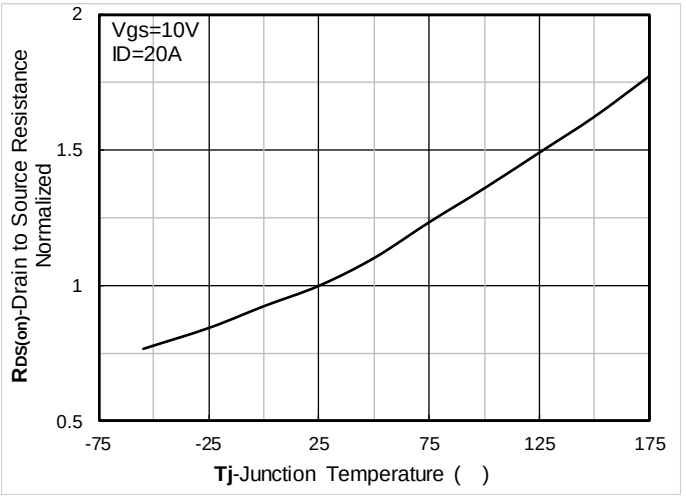



Figure 6. Normalized On-Resistance

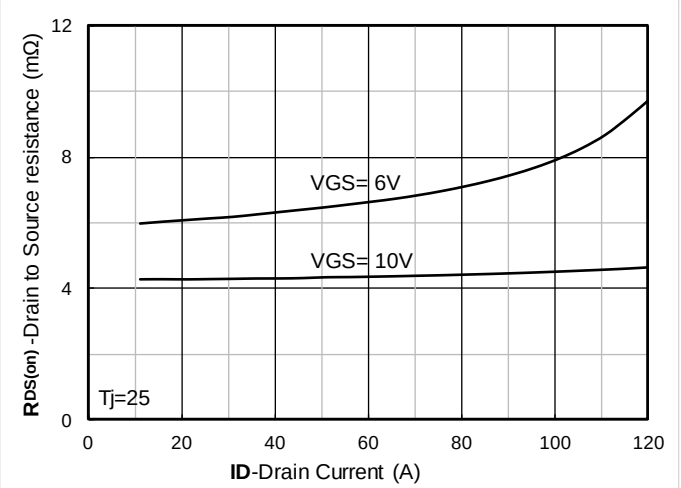



Figure 7. $R_{DS(on)}$ VS Drain Current

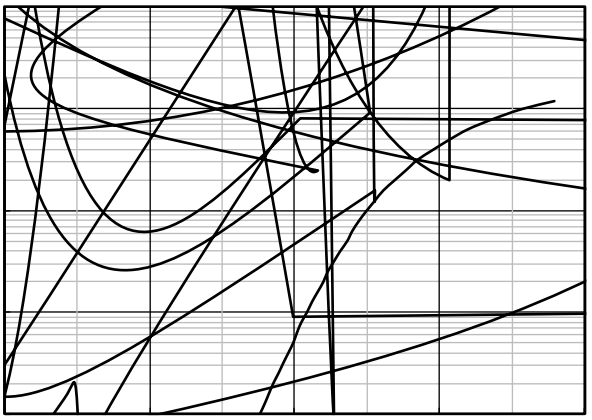


Figure 8. Forward characteristics of reverse diode

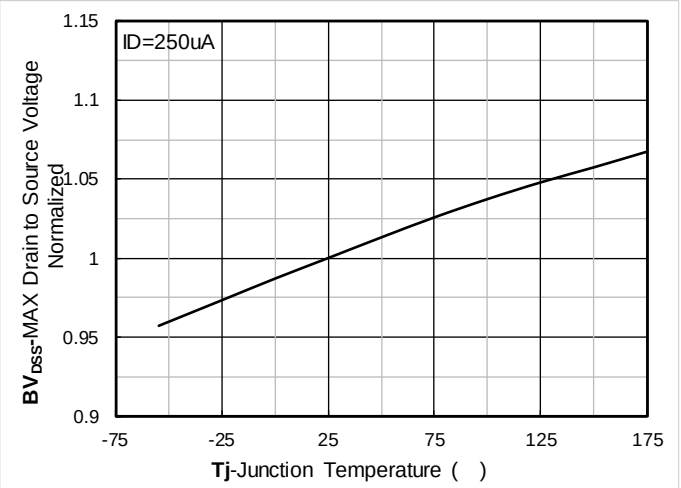



Figure 9. Normalized breakdown voltage

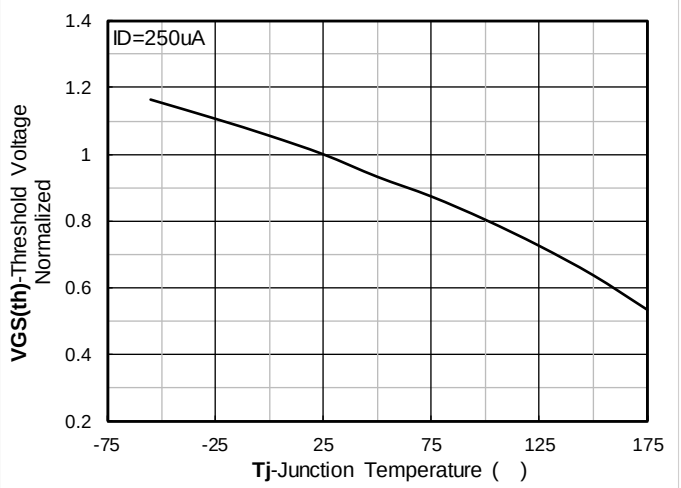



Figure 10. Normalized Threshold voltage

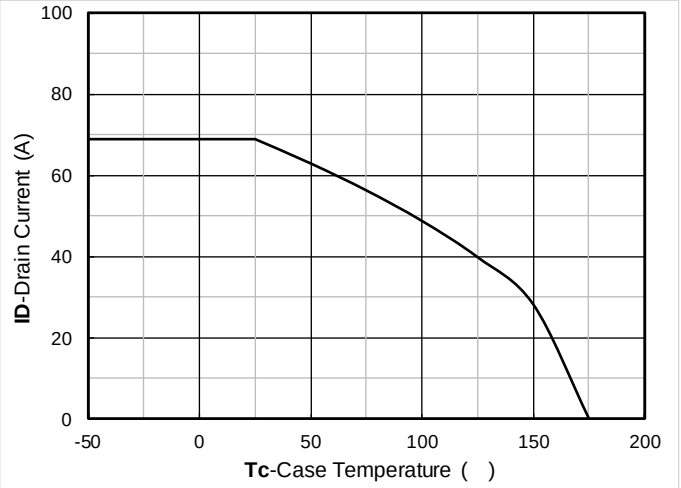



Figure 11. Current dissipation

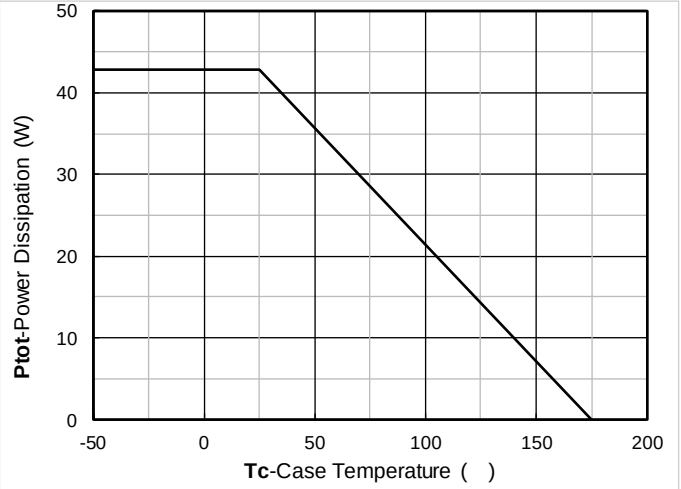



Figure 12. Power dissipation

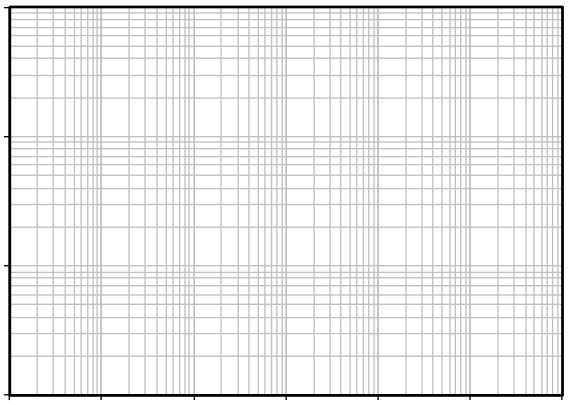


Figure 13. Maximum Transient Thermal Impedance

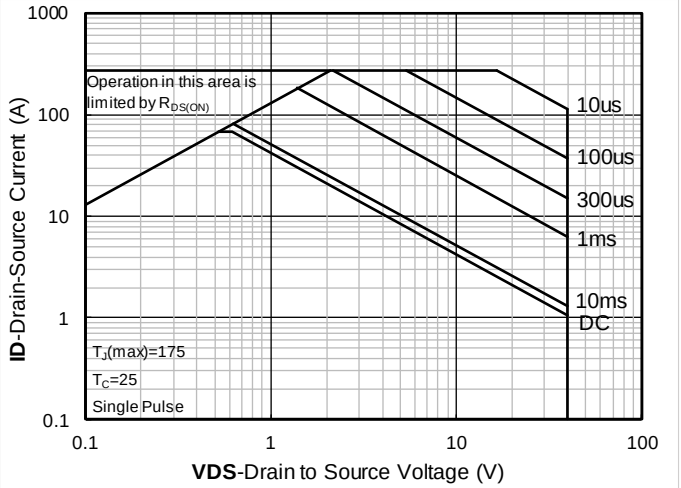



Figure 14. Safe Operation Area

## ■ Test Circuits & Waveforms

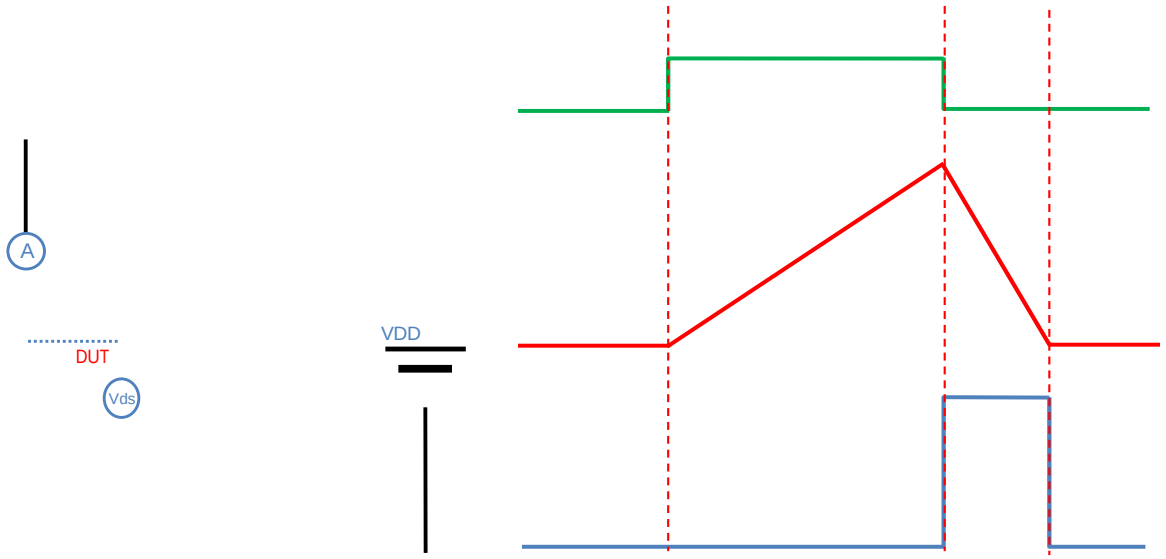



Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

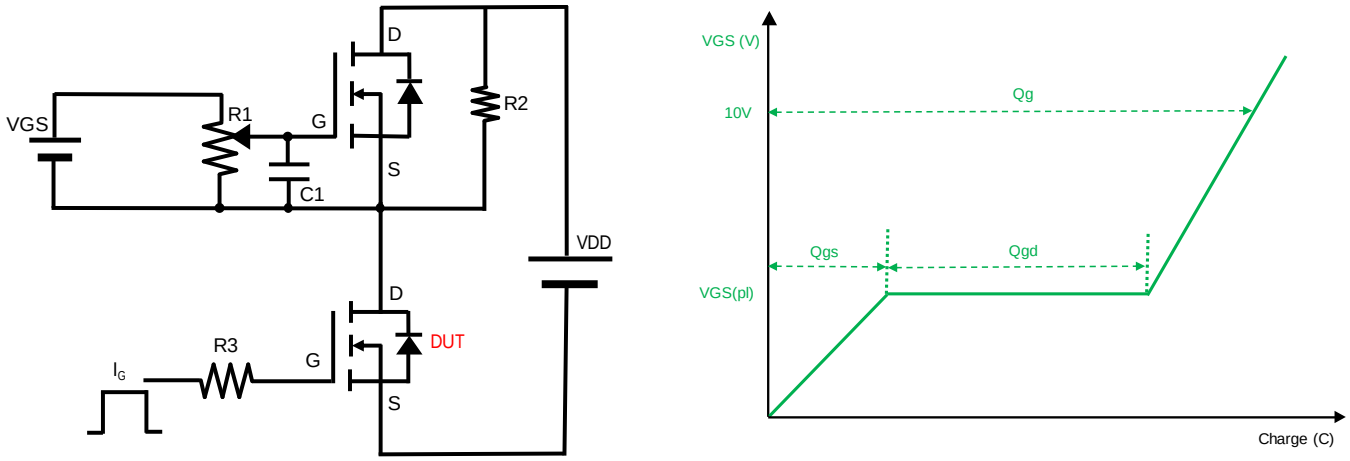



Figure B. Gate Charge Test Circuit & Waveform

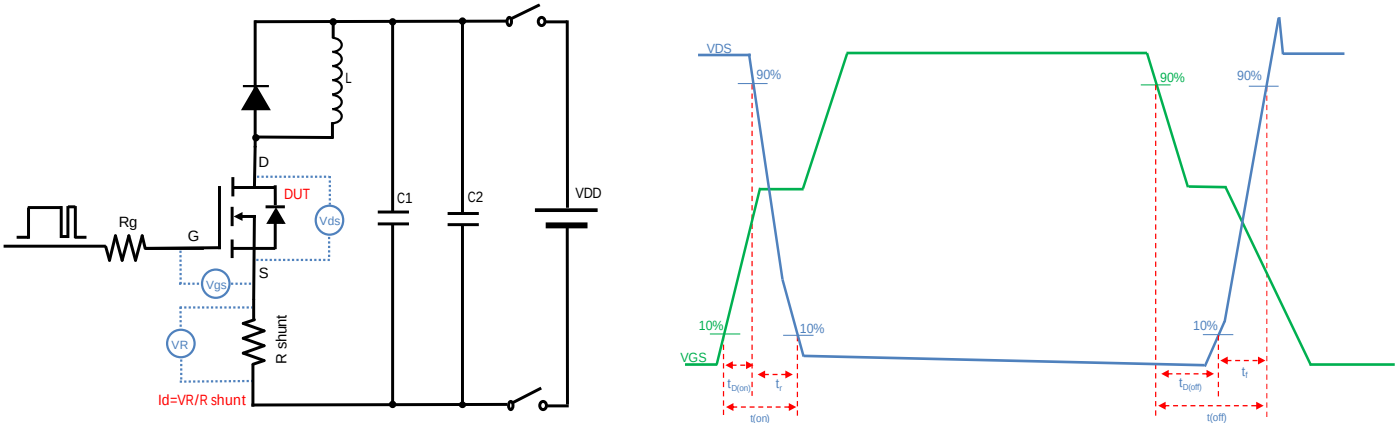



Figure C. Resistive Switching Test Circuit & Waveform

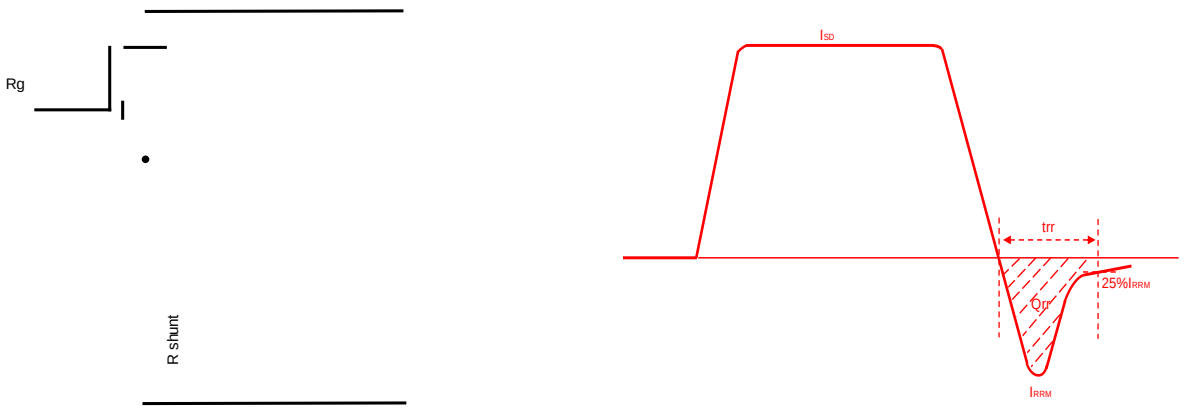
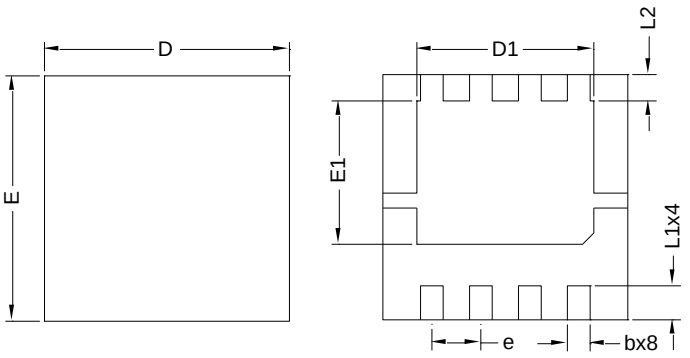


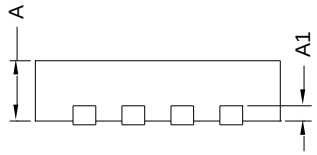

Figure D. Diode Recovery Test Circuit & Waveform

## ■ DFN3333-8L-A-0.8MM Package information

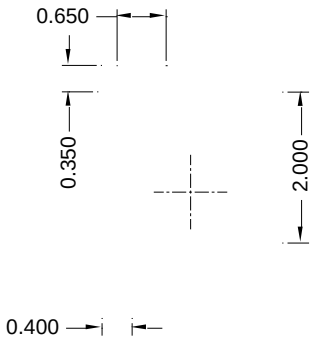



Top View　　Bottom View

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| D | 3.15 | 3.25 | 3.35 |
| E | 3.15 | 3.25 | 3.35 |
| A | 0.70 | 0.80 | 0.90 |
| A1 | | 0.20 BSC | |
| A2 | | | |




Side View




Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

## Disclaimer

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