■ PMOS Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V	-	-	-1	μA
		V_{DS}=-30V, V_{GS}=0V, Tj=150	-	-	-100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.0	-1.5	-2.4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V, I_D=-10A	-	31	40	mΩ
		V_{GS}=-4.5V, I_D=-5A	-	45	60	
Diode Forward Voltage	V_{SD}	I_S=-10A, V_{GS}=0V	-	-	-1.2	V
Gate resistance	R_G	f=1MHz	-	15	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	-20	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V, V_{GS}=0V, f=1MHz	-	490	-	pF
Output Capacitance	C_{oss}		-	75	-	
Reverse Transfer Capacitance	C_{rss}		-	60	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V, V_{DS}=-15V, I_D=-10A	-	9	-	nC
Gate-Source Charge	Q_{gs}		-	2.5	-	
Gate-Drain Charge	Q_{gd}		-	2.3	-	
Reverse Recovery Charge	Q_{rr}	I_F=-10A, di/dt=100A/us	-	15	-	nC
Reverse Recovery Time	t_{rr}		-	35	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DD}=-15V, ID=-10A R_{GEN}=2.5Ω	-	9	-	ns
Turn-on Rise Time	t_r		-	3.5	-	
Turn-off Delay Time	$t_{D(off)}$		-	30	-	
Turn-off fall Time	t_f		-	18	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. NMOS: T_J=25℃, V_{DD}=25V, V_{GS}=10V, R_G=25Ω, L=0.5mH, IAS=8A.
PMOS: T_J=25℃, V_{DD}=-25V, V_{GS}=-10V, R_G=25Ω, L=0.5mH, IAS=-8A.
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in the still air environment with T_A =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

NMOS Typical Electrical and Thermal Characteristics Diagrams

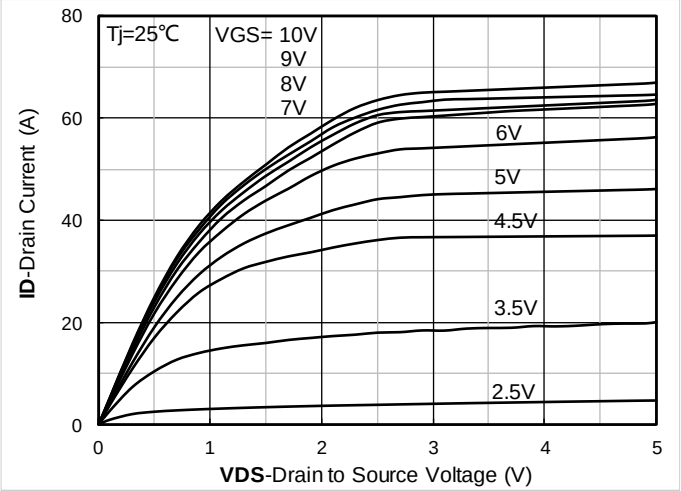


Figure 1. Output Characteristics

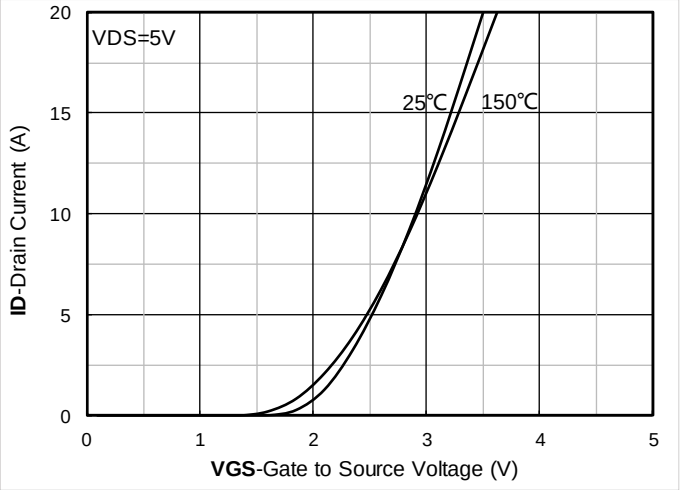


Figure 2. Transfer Characteristics

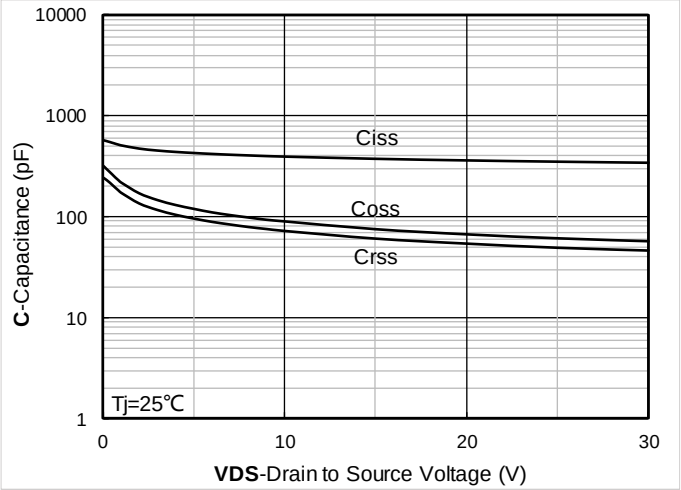


Figure 3. Capacitance Characteristics

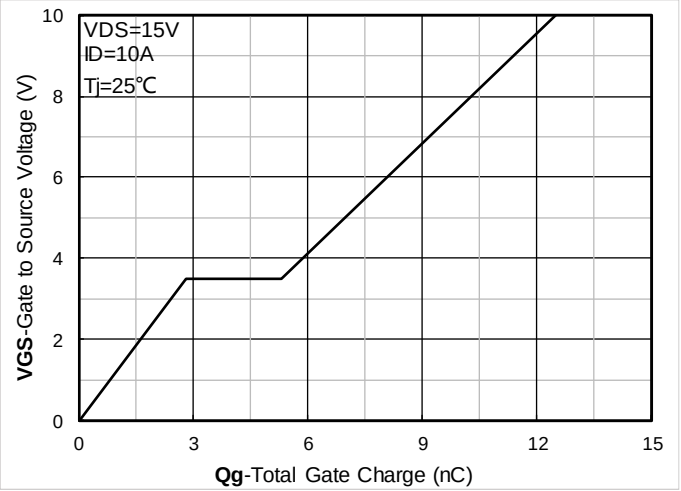


Figure 4. Gate Charge

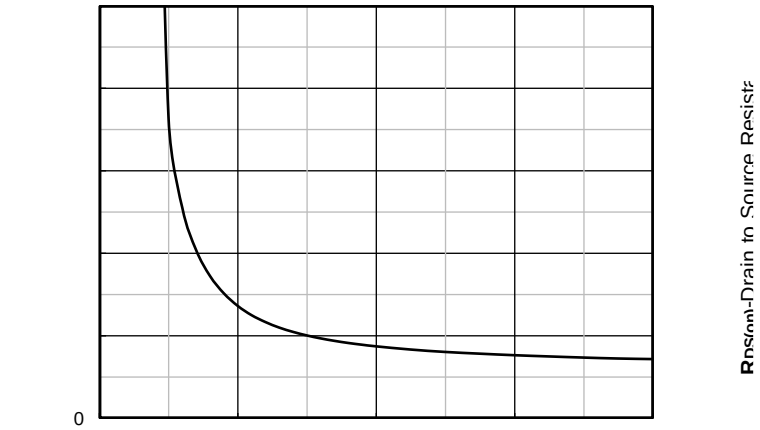


Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On- Resistance

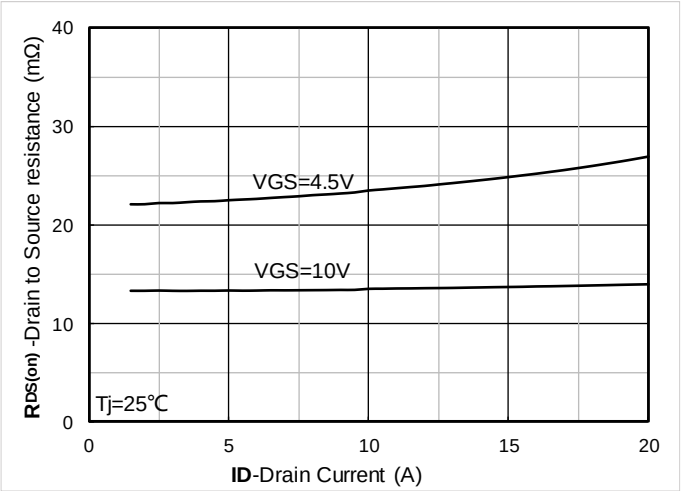


Figure 7. $R_{DS(on)}$ VS Drain Current

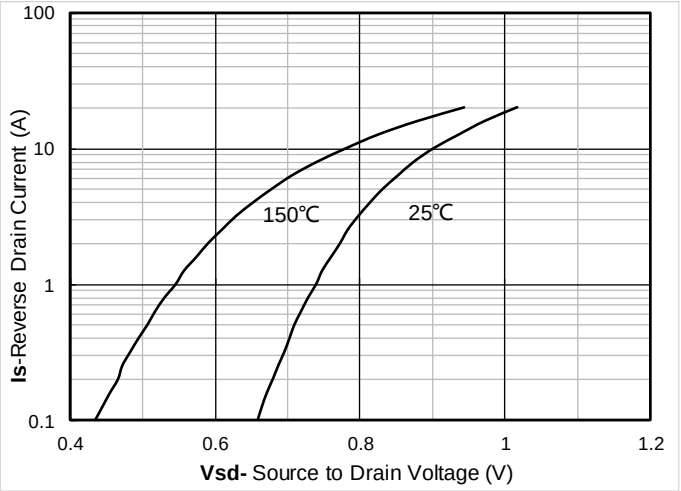


Figure 8. Forward characteristics of reverse diode

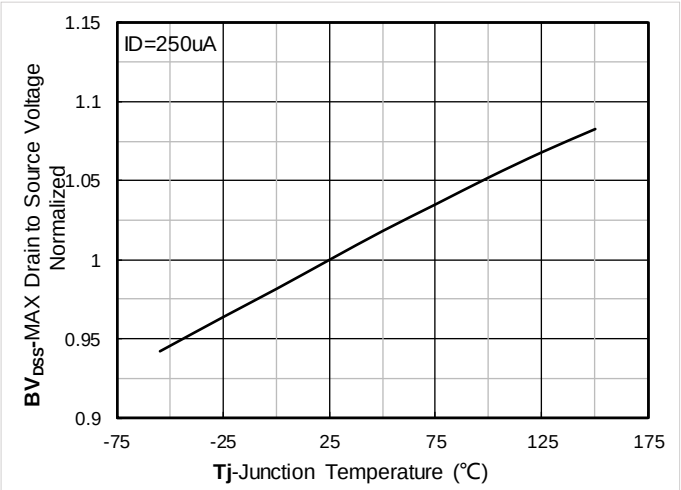


Figure 9. Normalized breakdown voltage

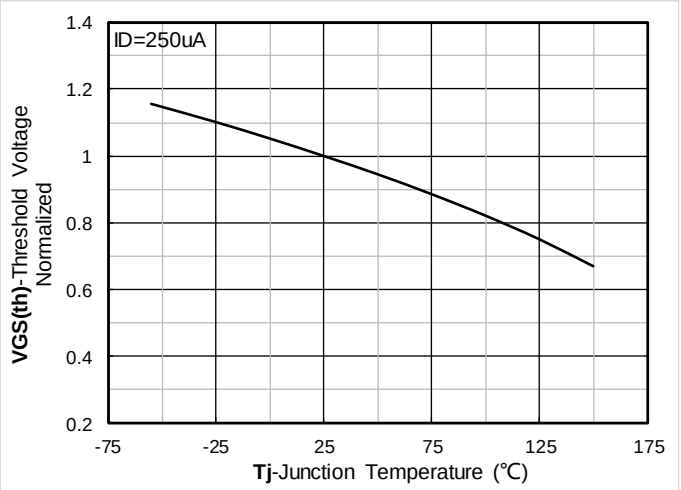


Figure 10. Normalized Threshold voltage

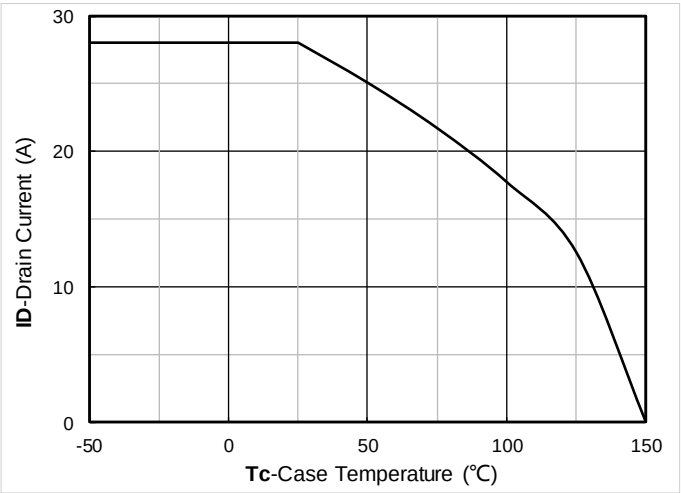


Figure 11. Current dissipation

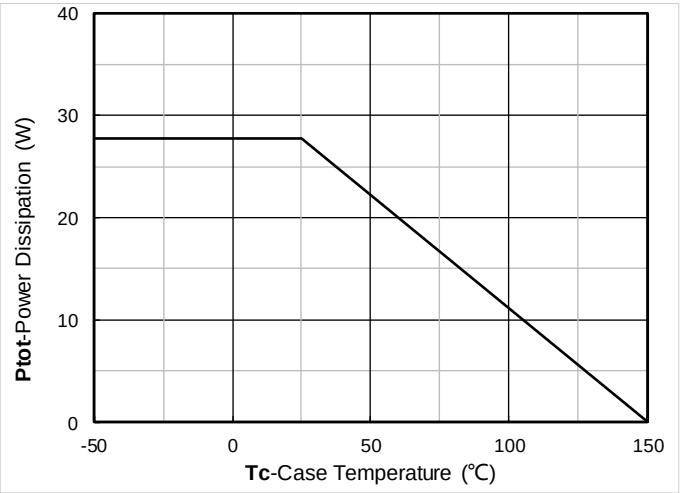


Figure 12. Power dissipation

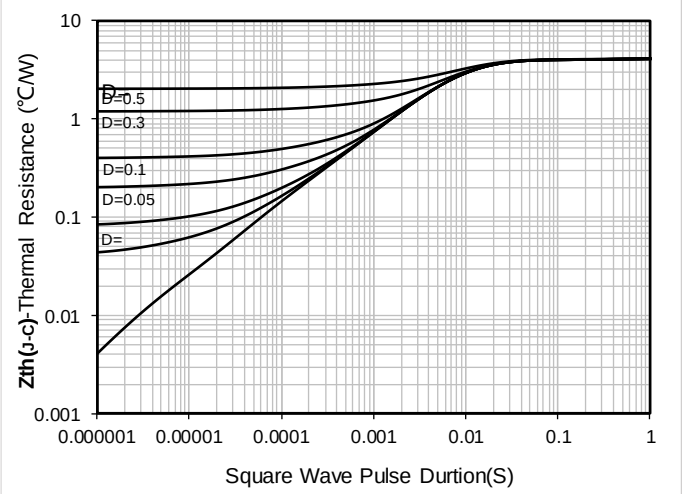


Figure 13. Maximum Transient Thermal Impedance

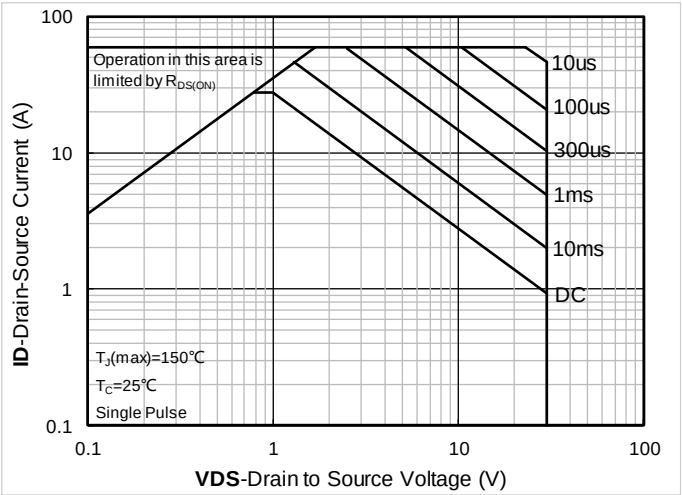


Figure 14. Safe Operation Area

PMOS Typical Electrical and Thermal Characteristics Diagrams

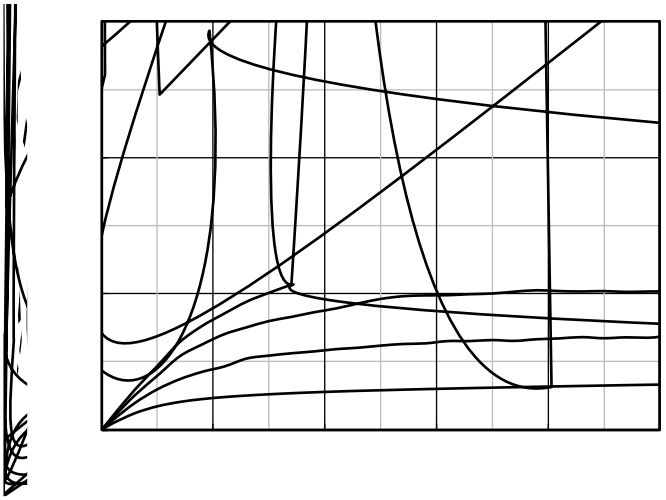


Figure 1. Output Characteristics

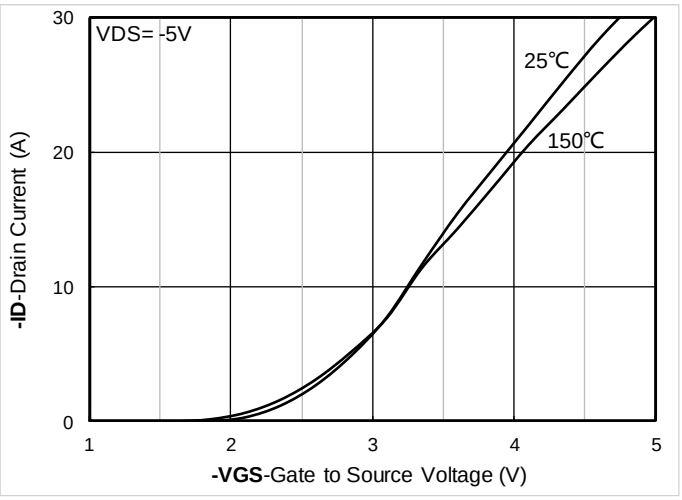


Figure 2. Transfer Characteristics

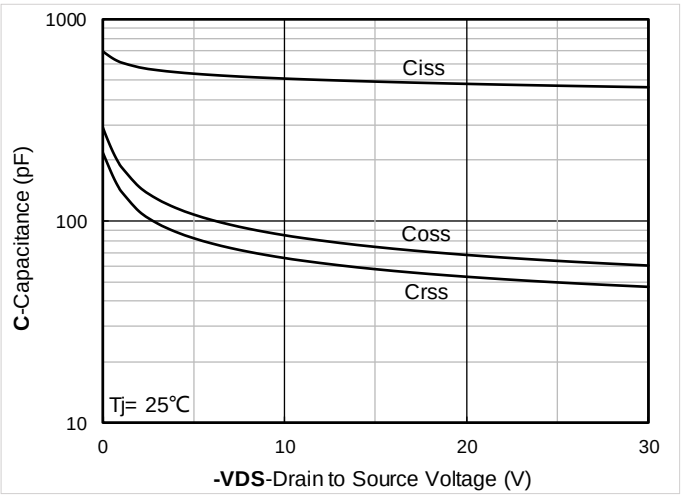


Figure 3. Capacitance Characteristics

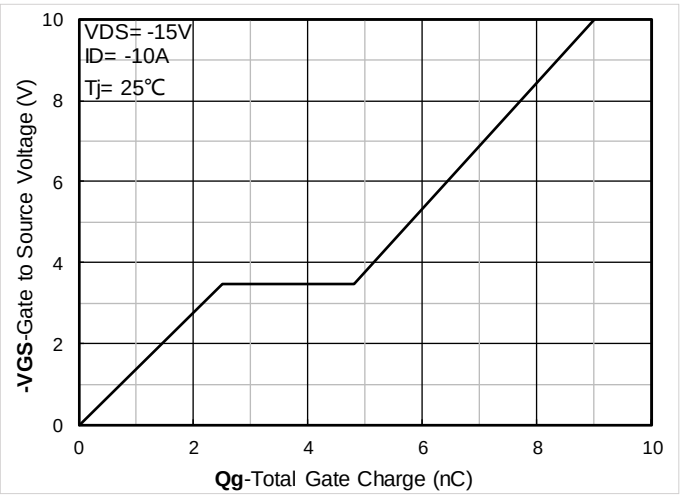


Figure 4. Gate Charge

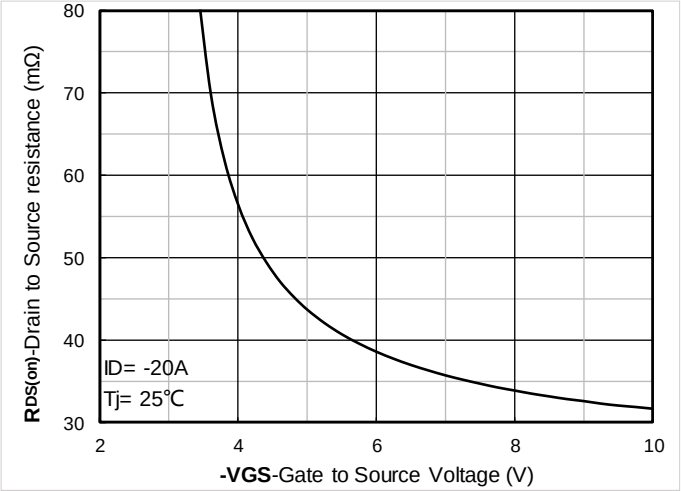


Figure 5. On-Resistance vs Gate to Source Voltage

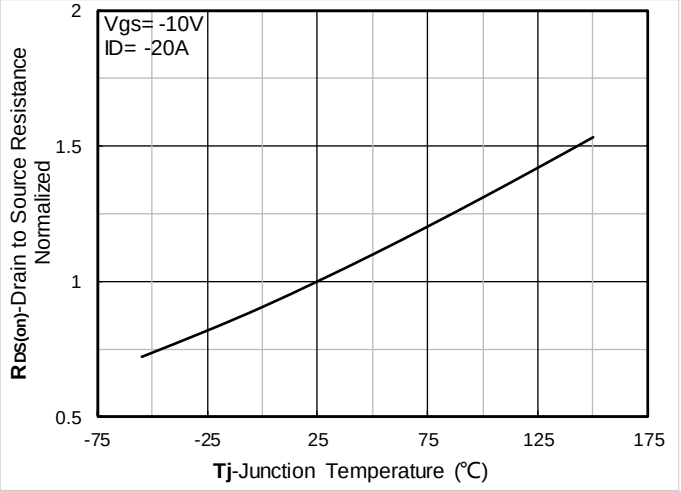


Figure 6. Normalized On-Resistance

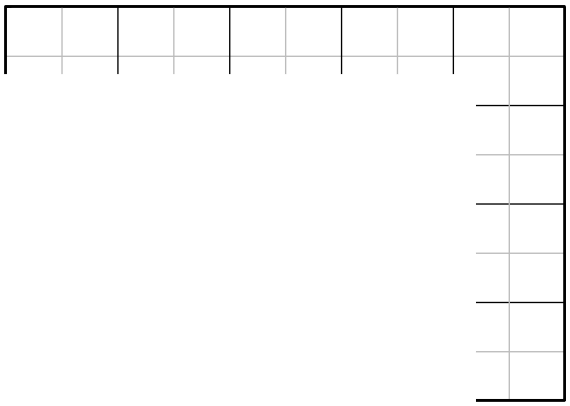


Figure 7. $R_{DS(on)}$ VS Drain Current

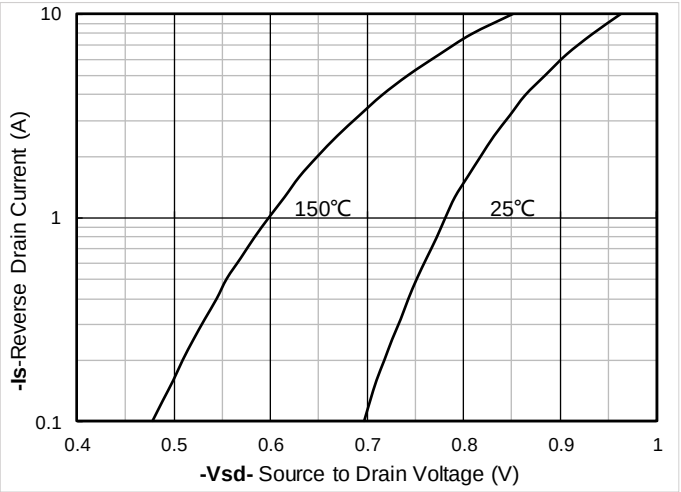


Figure 8. Forward characteristics of reverse diode

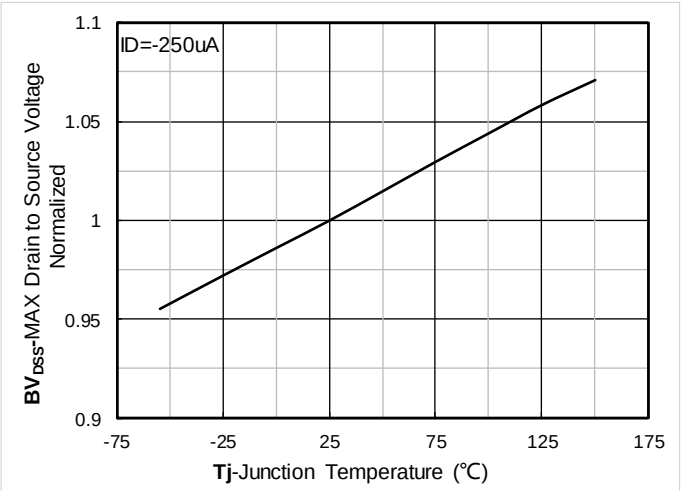


Figure 9. Normalized breakdown voltage

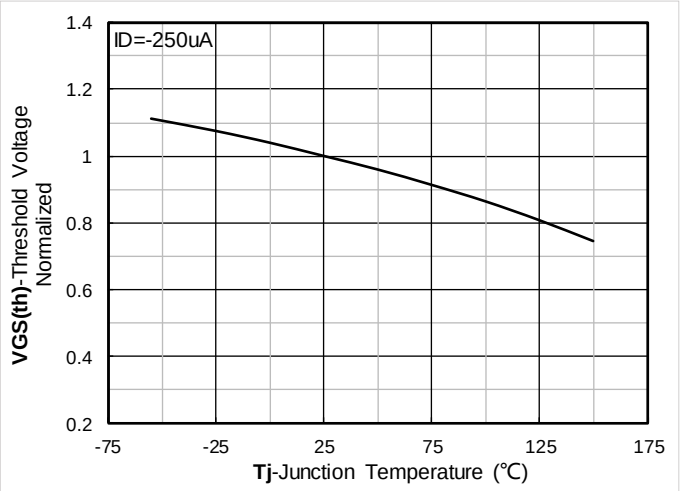


Figure 10. Normalized Threshold voltage

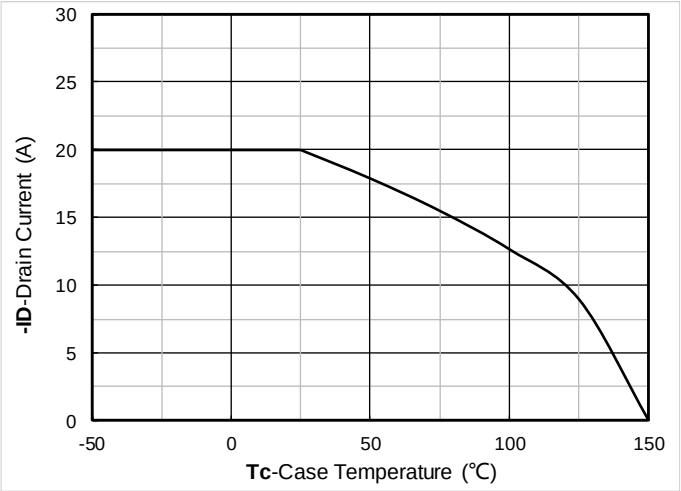


Figure 11. Current dissipation

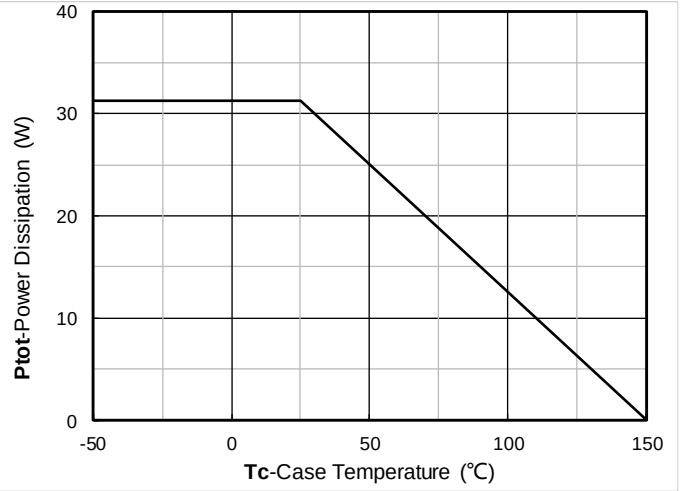


Figure 12. Power dissipation

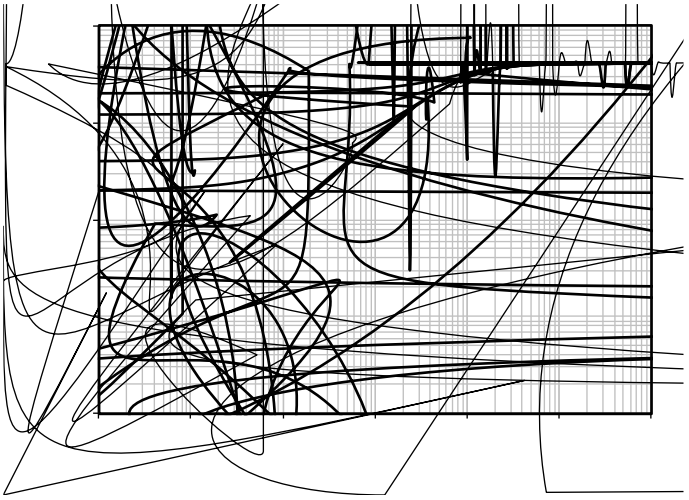


Figure 13. Maximum Transient Thermal Impedance

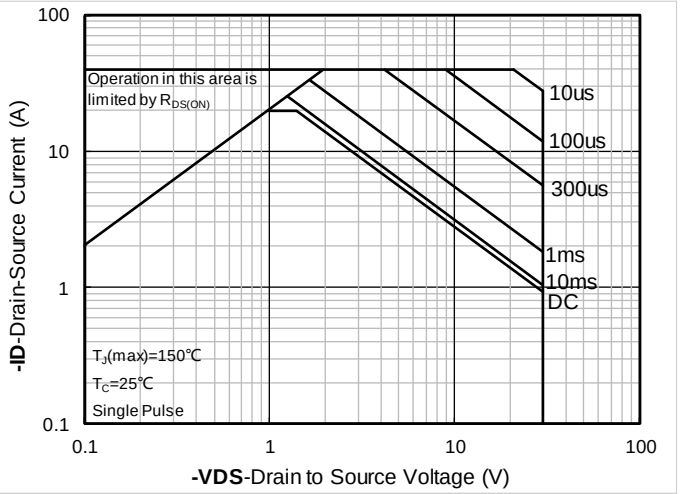
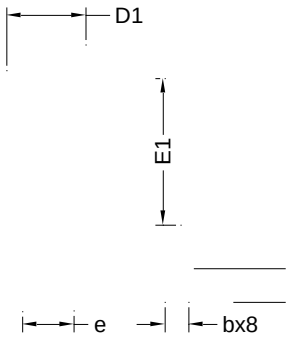
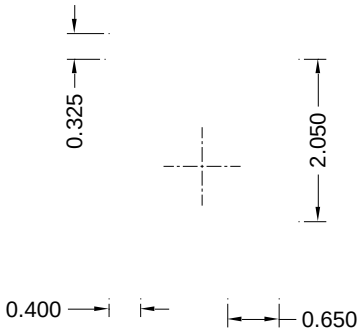


Figure 14. Safe Operation Area

■ DFN3333-8L-B-0.8MM Package information





Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

Disclaimer