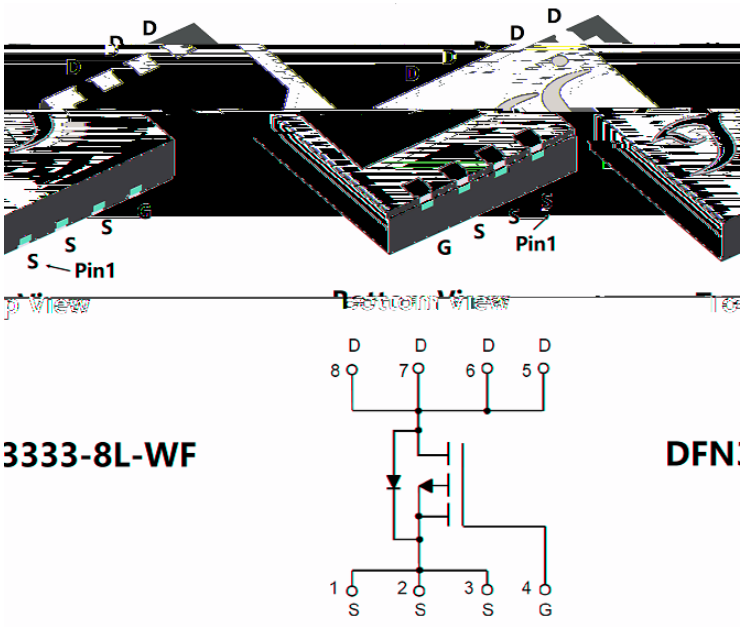
P-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} -100V
- I_D -15A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜120mΩ
- 100% EAS Tested
- 100% ▽V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power management
- Portable equipment

■ Absolute Maximum Ratings (T_J=25℃ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	-100	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25 , V_{GS}= -10V	I_D	-2.8	A
		T_A=100 , V_{GS}= -10V		-2	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25 , V_{GS}= -10V		-15	
		T_C =100 , V_{GS}= -10V		-10.6	
Pulsed Drain Current	T_C=25℃, t_p=100μs		I_{DM}	-45	A
Avalanche energy	V_G=-10V, R_G=25Ω, L=1mH, IAS=-12.9A		EAS	83.2	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25	P_D	2	W
		T_A=100		1	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25		56	
		T_C =100		28	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55～+175	

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	60	75	/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2.2	2.65	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ120GP10HHQ	F1	120GP10H	5000	10000	100000	13" reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V, V_{GS}=0V	-	-	-1	μA
		V_{DS}=-100V, V_{GS}=0V, Tj=125	-	-	-100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-2.0	-2.7	-3.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-15A	-	84	120	mΩ
Diode Forward Voltage	V_{SD}	I_S=-15A, V_{GS}=0V	-	-	-1.2	V
Gate resistance	R_G	f=1MHz	-	12	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	-15	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-50V, V_{GS}=0V, f=1MHz	-	900	-	pF
Output Capacitance	C_{oss}		-	110	-	
Reverse Transfer Capacitance	C_{rss}		-	6.3	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V, V_{DS}=-50V, I_D=-15A	-	15.5	-	nC
Gate-Source Charge	Q_{gs}		-	2.6	-	
Gate-Drain Charge	Q_{gd}		-	2.2	-	
Reverse Recovery Charge	Q_{rr}	I_F=-15A, di/dt=100A/us	-	112	-	nC
Reverse Recovery Time	t_{rr}		-	47	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DD}=-50V, I_D=-15A R_{GEN}=3Ω	-	8	-	ns
Turn-on Rise Time	t_r		-	58	-	
Turn-off Delay Time	$t_{D(off)}$		-	27	-	
Turn-off fall Time	t_f		-	13.5	-	

Note：

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with TA =25℃.The maximum allowed junction temperature of 175℃. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams

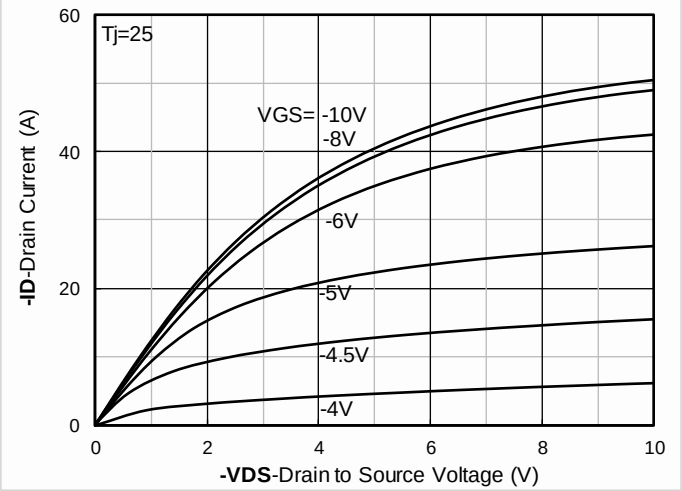


Figure 1. Output Characteristics

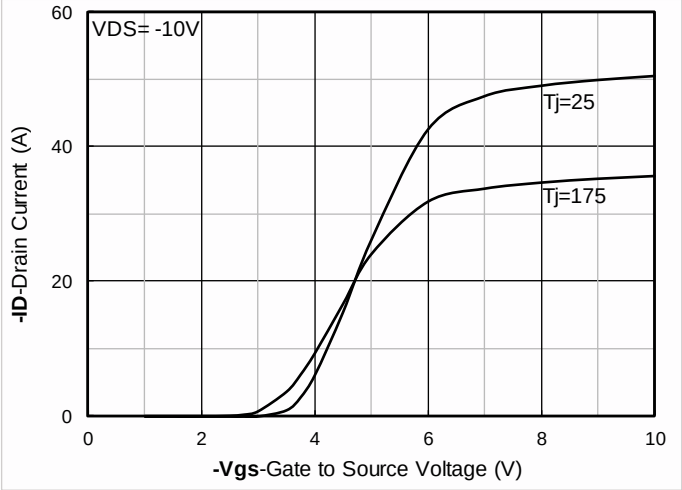


Figure 2. Transfer Characteristics

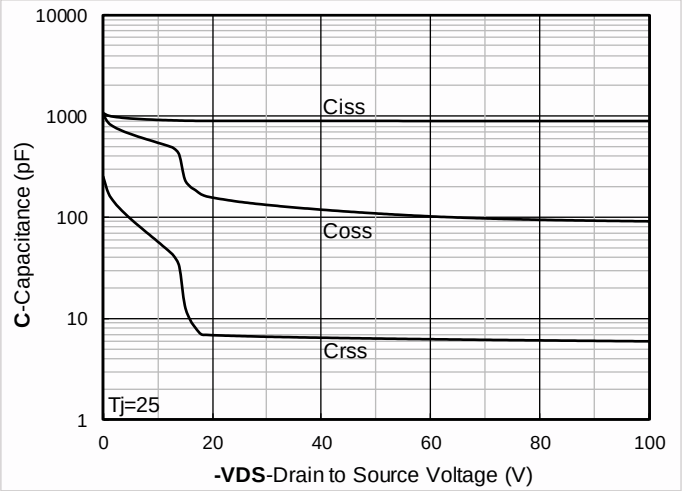


Figure 3. Capacitance Characteristics

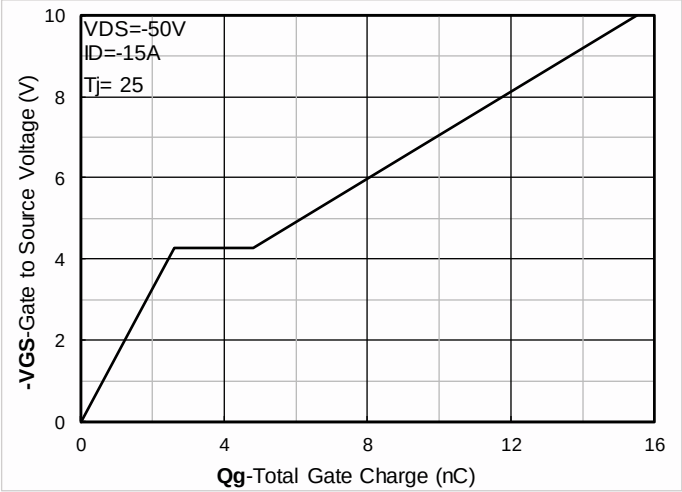
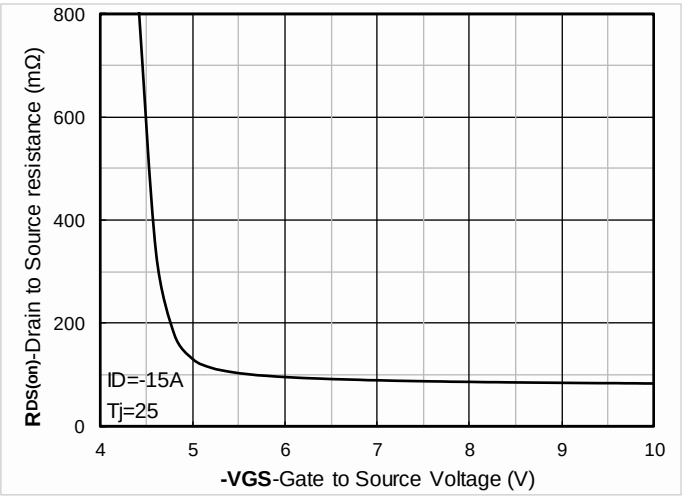
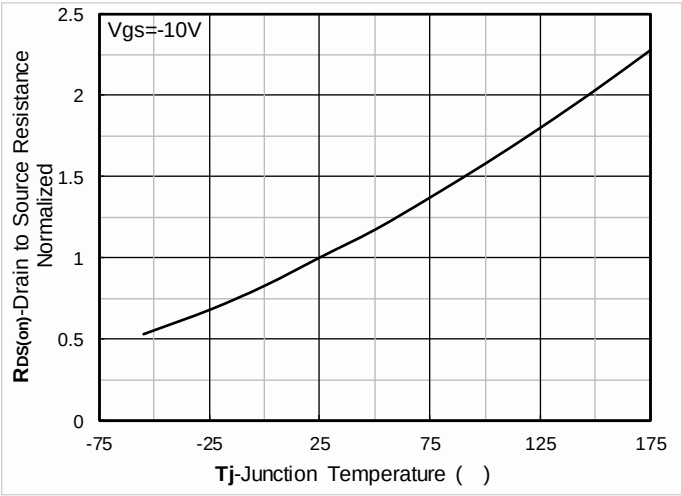


Figure 4. Gate Charge





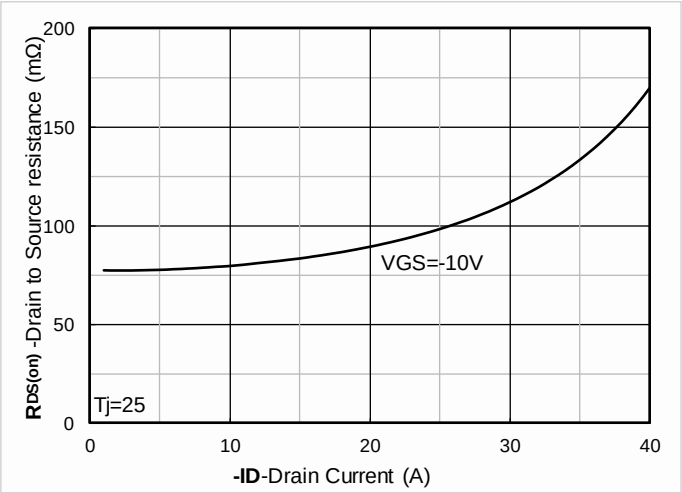


Figure 7. $R_{DS(on)}$ VS Drain Current

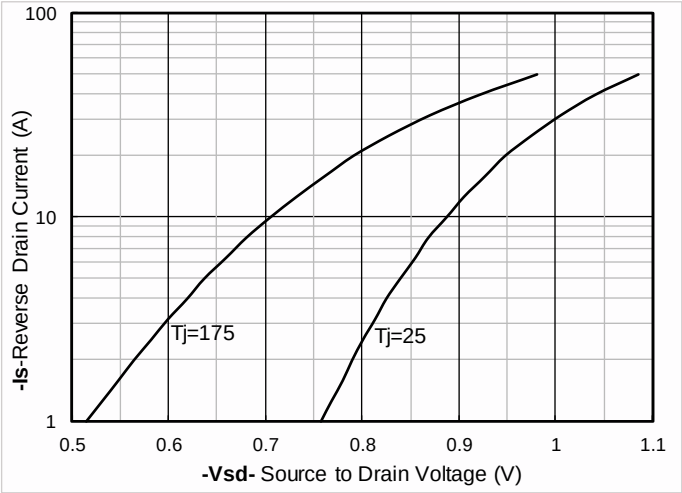


Figure 8. Forward characteristics of reverse diode

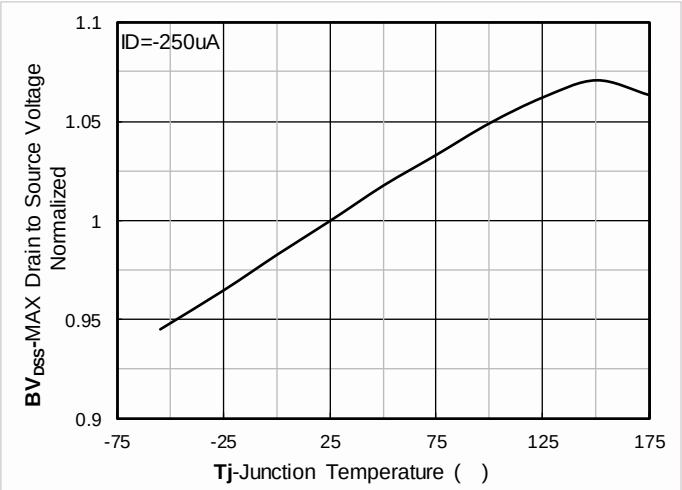


Figure 9. Normalized breakdown voltage

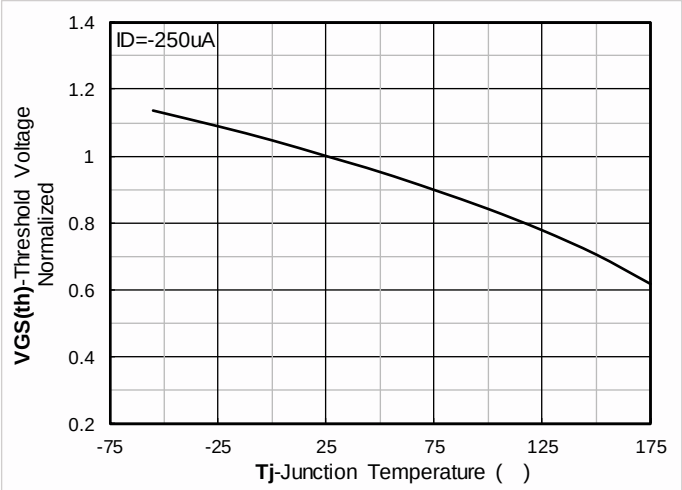


Figure 10. Normalized Threshold voltage

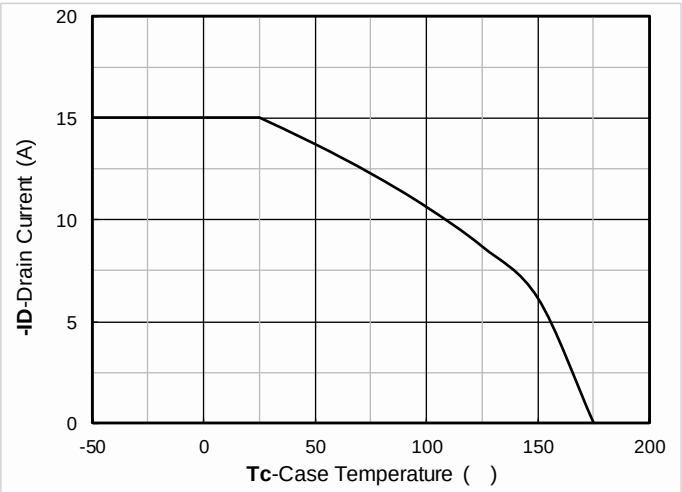


Figure 11. Current dissipation

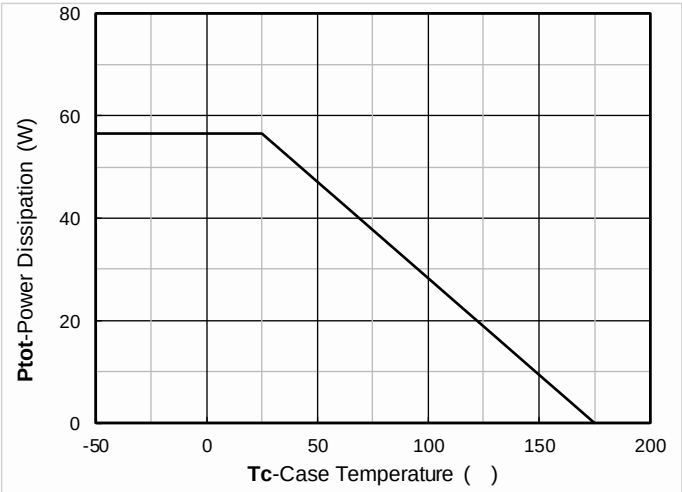
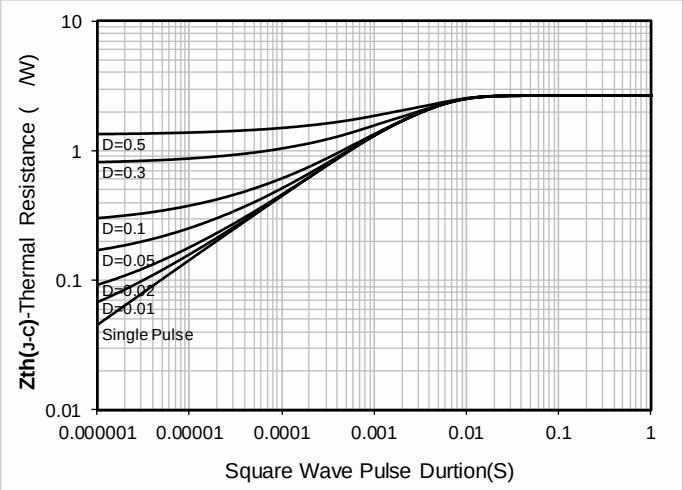
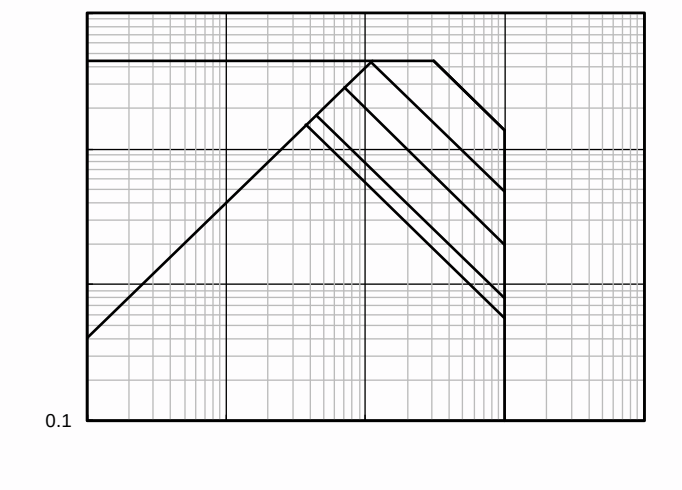


Figure 12. Power dissipation


10
1
0.1
0.01
Zth(j-c)-Thermal Resistance (/W)
D=0.5
D=0.3
D=0.1
D=0.05
D=0.02
D=0.01
Single Pulse
0.000001
0.00001
0.0001
0.001
0.01
0.1
1
Square Wave Pulse Durtion(S)


0.1

[redacted]

■ **DFN3333-8L-WF Package information**

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