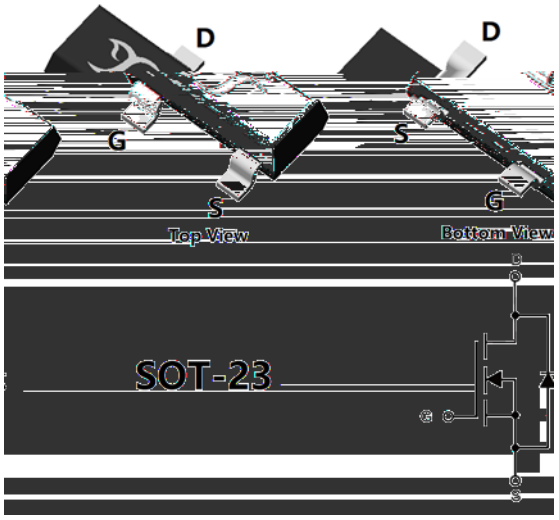
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	60V
I_D	3.0A
$R_{DS(ON)}$(at V_{GS}=10V)	100mohm
$R_{DS(ON)}$(at V_{GS}=4.5V)	120mohm

/. . ▽V_{DS} Tested

General Description

Trench Power MV MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Fre

Applications

DC-DC Converters
Power management functions

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Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	20	V
Drain Current	T_A=25	I_D	3	A
	T_A=70		2.4	
Pulsed Drain Current [A]		I_{DM}	12	A
Total Power Dissipation	T_A=25	P_D	1.2	W
	T_A=70		0.8	W
Thermal Resistance Junction-to-Ambient [B]		R_{JA}	104	/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL03N06A	F2	S10	3000	30000	120000	7 reel

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	
Gate-Body Leakage Current	I_{GSS1}	V_{GS}= 20V, V_{DS}=0V			100	nA
	I_{GSS2}	V_{GS}= 10V, V_{DS}=0V			50	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250	0.9	1.3	2.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=3A		86	100	m
		V_{GS}=4.5V, I_D=2A		92	120	
Diode Forward Voltage	V_{SD}	I_S=3A,V_{GS}=0V			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}			409		
Output Capacitance	C_{oss}	V_{DS}=10V,V_{GS}=0V,f=1MHZ		50		pF

Typical Performance Characteristics

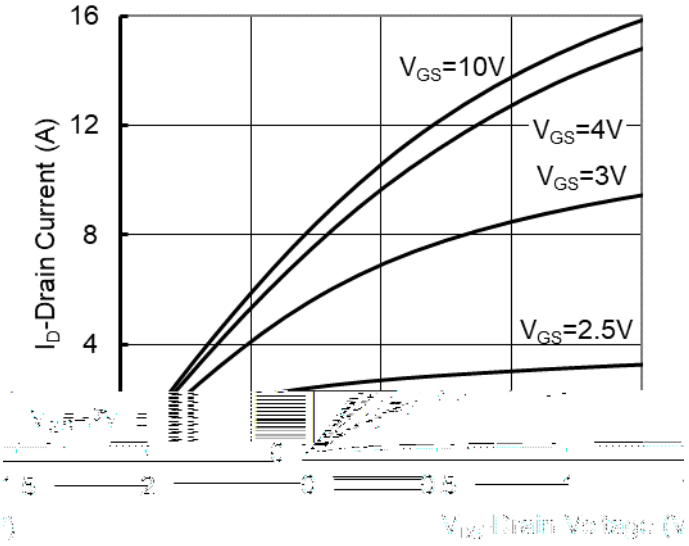


Figure1. Output Characteristics

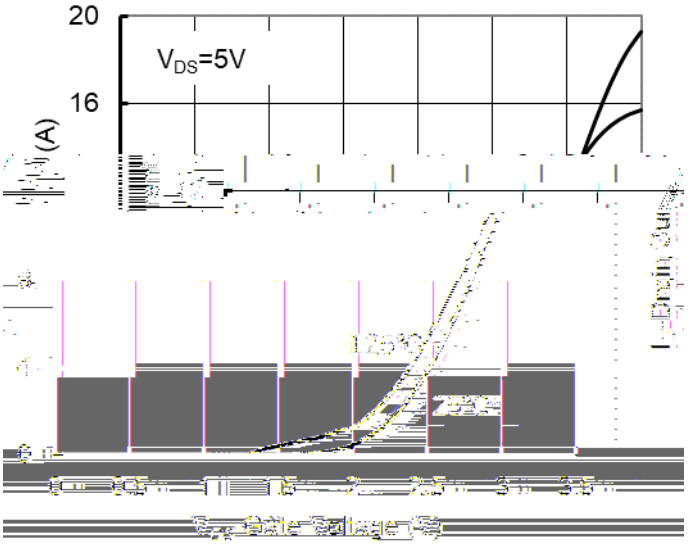


Figure2. Transfer Characteristics

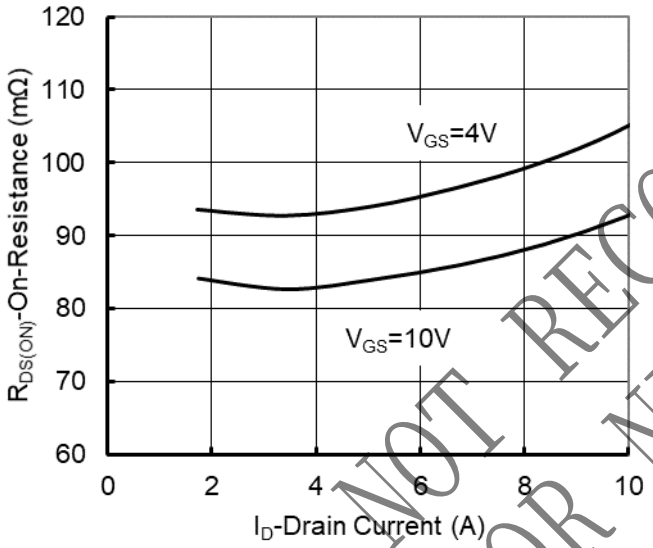


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

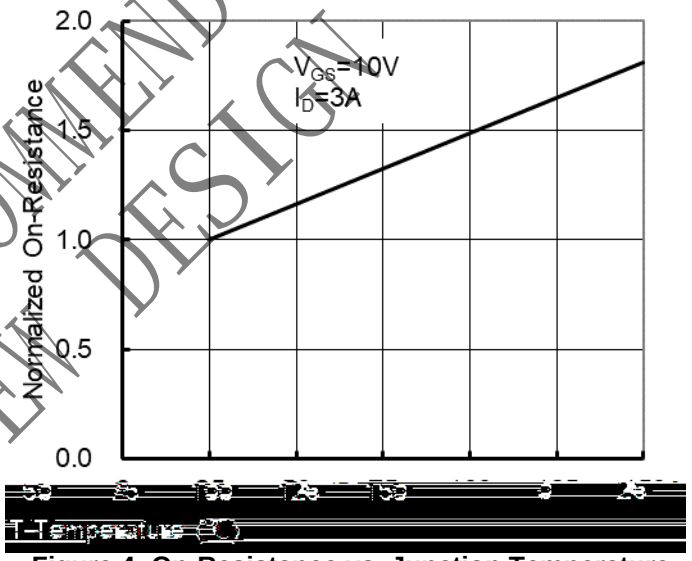


Figure 4: On-Resistance vs. Junction Temperature

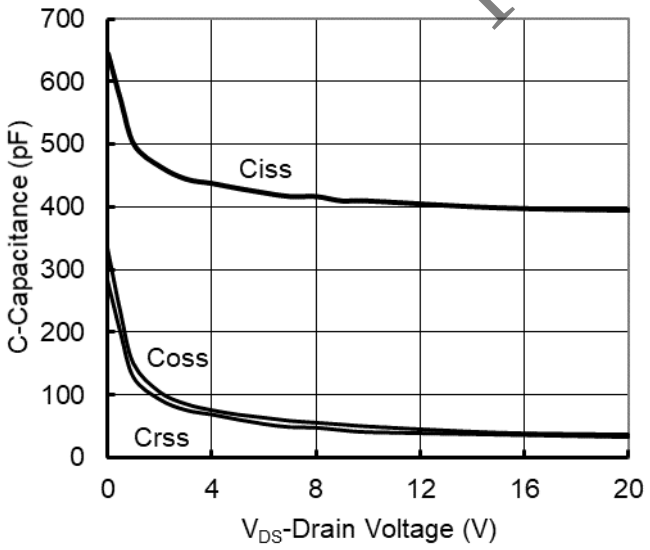


Figure5. Capacitance Characteristics

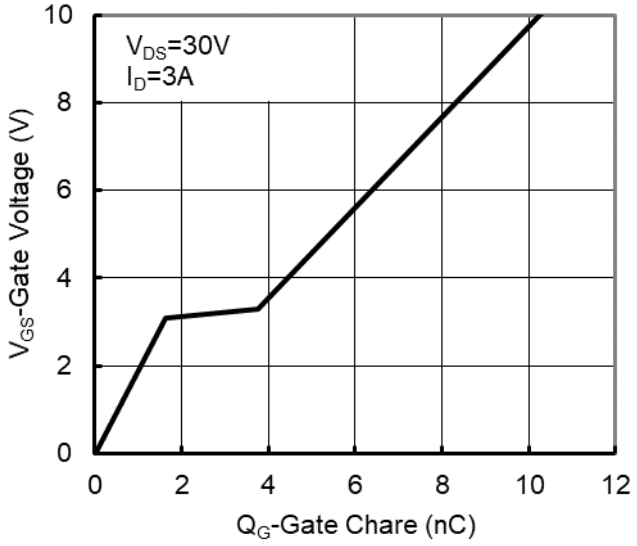


Figure6. Gate Charge

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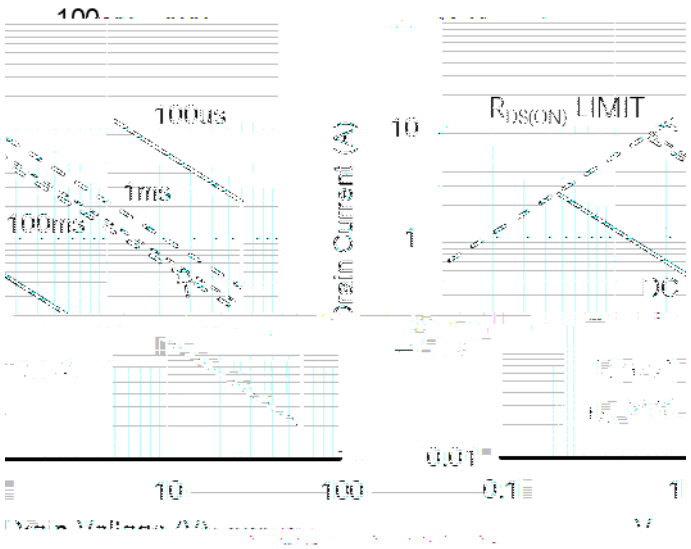


Figure7. Safe Operation Area

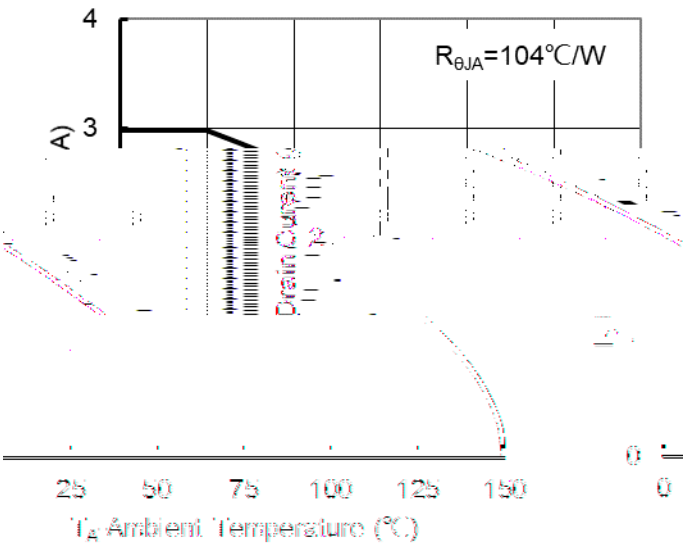


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

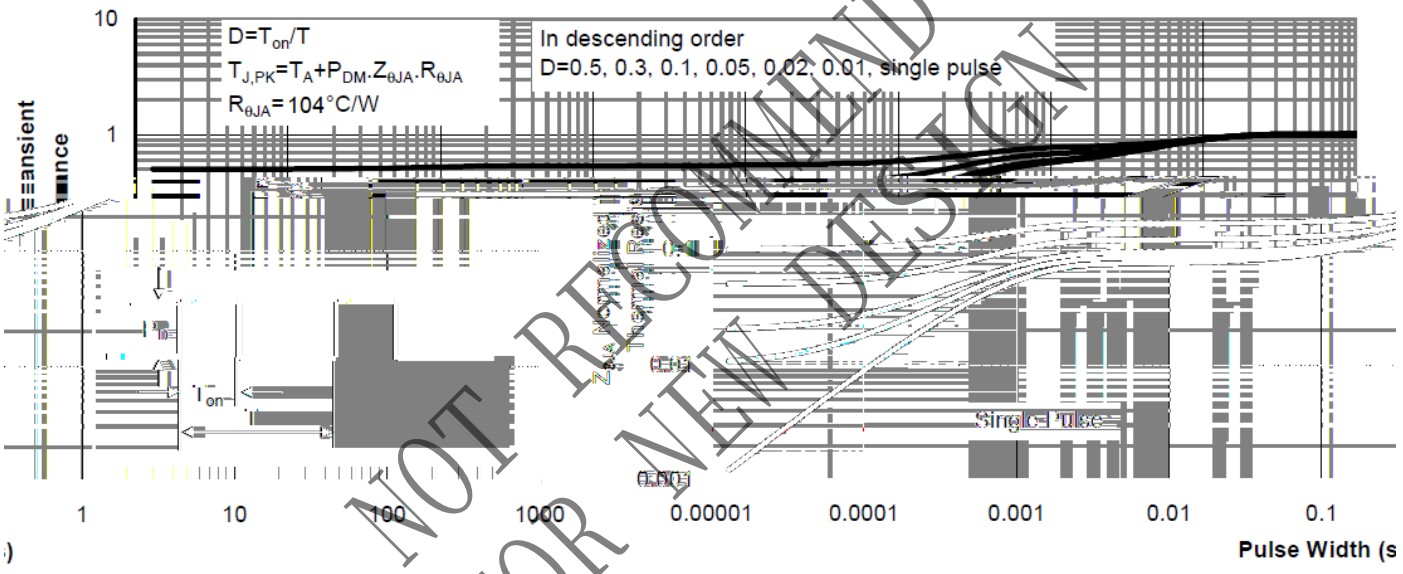


Figure9. Normalized Maximum Transient Thermal Impedance

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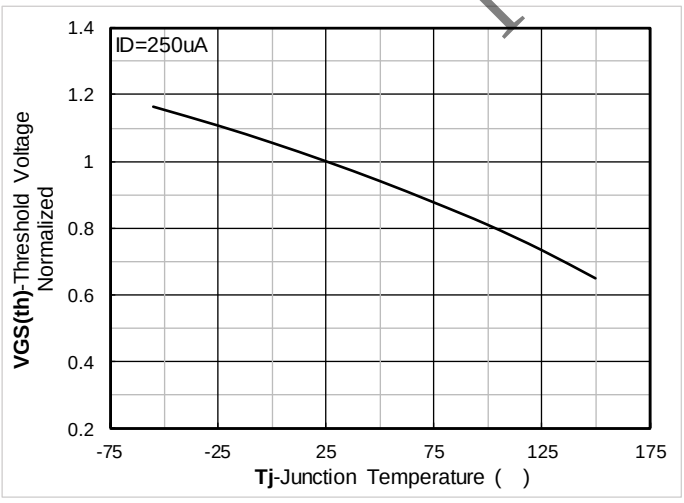
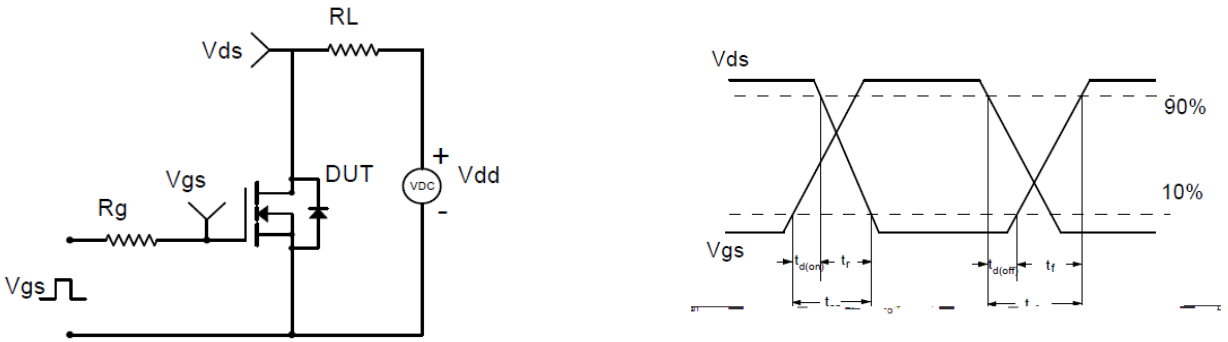
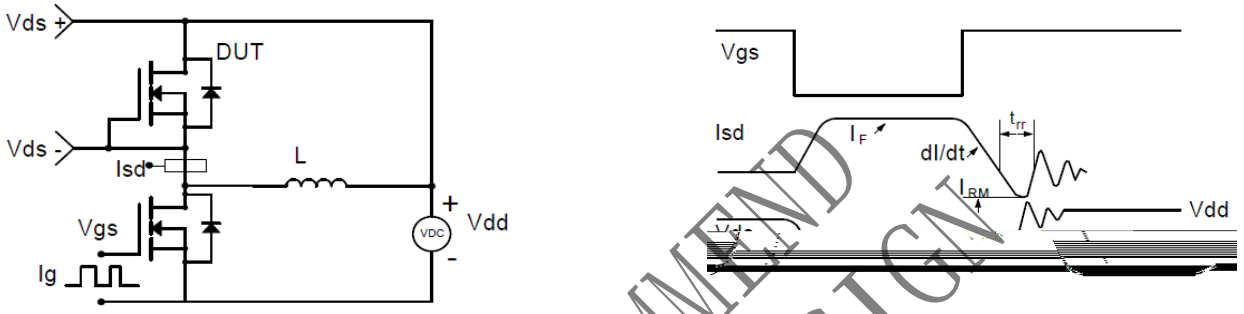


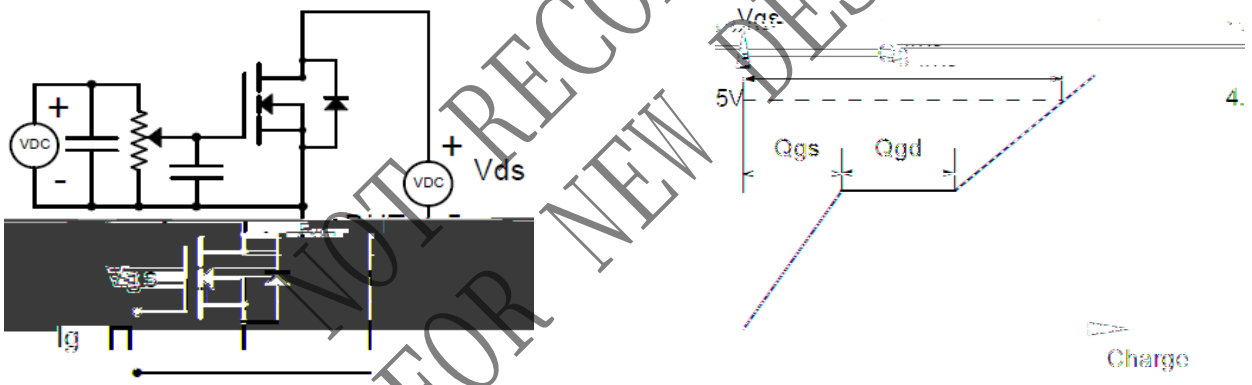
Figure 10. Normalized Threshold voltage



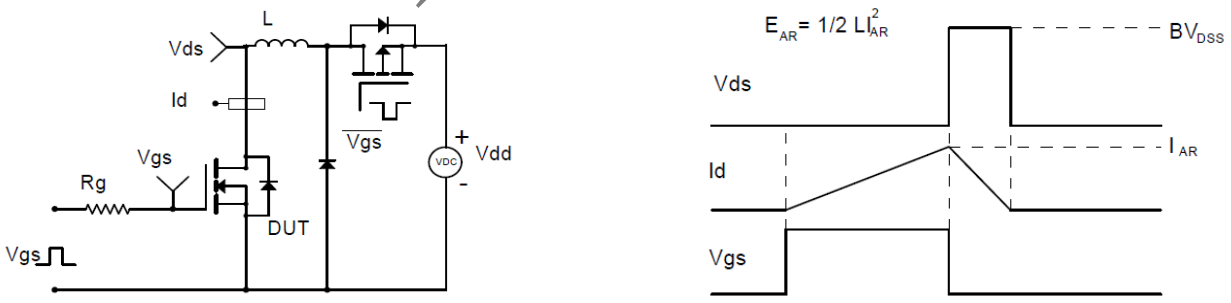
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

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