N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 40V
- I_D 2.5A
- $R_{DS(ON)}$(at V_{GS}=10V) 100mohm
- $R_{DS(ON)}$(at V_{GS}=6V) 140mohm
- ESD protected up to 2.0KV (HBM)

General Description

- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Moisture Sensitivity Level 1
- Part no. with suffix “Q” means AEC-Q101 qualified

Applications

- Battery operated systems
- Solid-state relays
- Direct logic-level interface TTL/CMOS
-

■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	40	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	2.5	A
Pulsed Drain Current [A]	I_{DM}	12	A
Total Power Dissipation @ T_A=25	P_D	1.1	W
Thermal Resistance Junction-to-Ambient @ Steady State [B]	$R_{\theta JA}$	110	W
Junction and Storage Temperature Range	T_J ,T_{STG}	-55 +150	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ± 20V, V_{DS}=0V			± 10	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V				

■ Typical Performance Characteristics

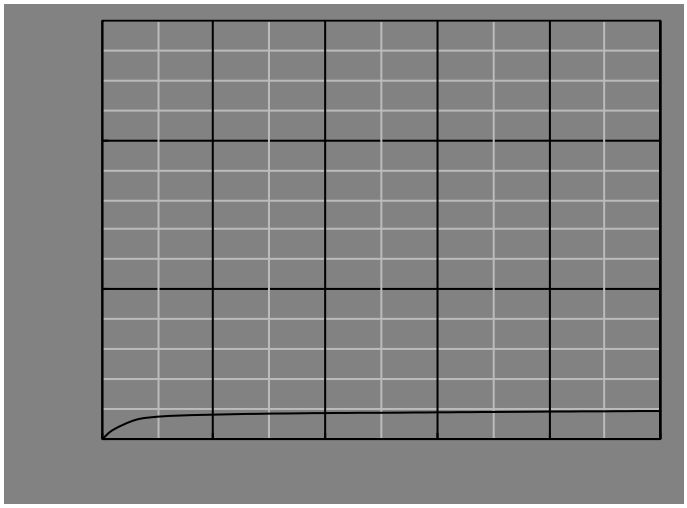


Figure1. Output Characteristics

Figure2. Transfer Characteristics

Figure3. Capacitance Characteristics

Figure4. Gate Charge

Figure5. On-Resistance vs Gate to Source Voltage

Figure6. Normalized On-Resistance

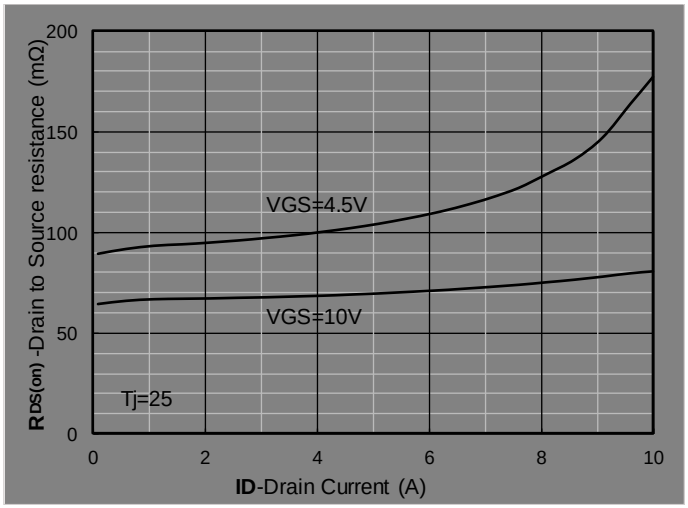


Figure 7. $R_{DS(on)}$ VS Drain Current

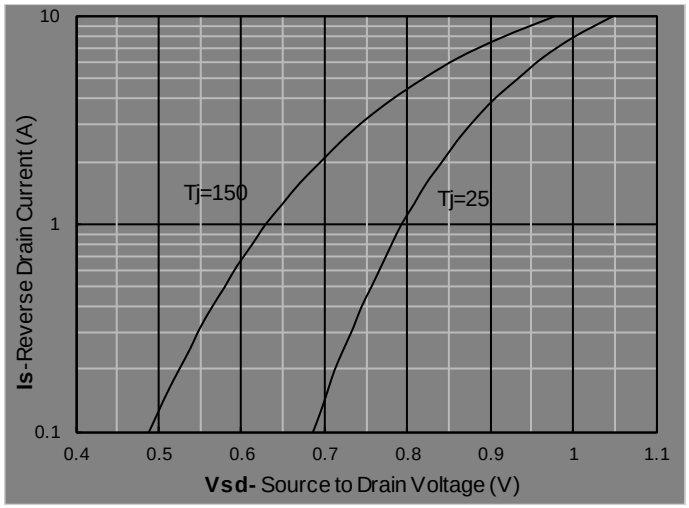


Figure 8. Forward characteristics of reverse diode

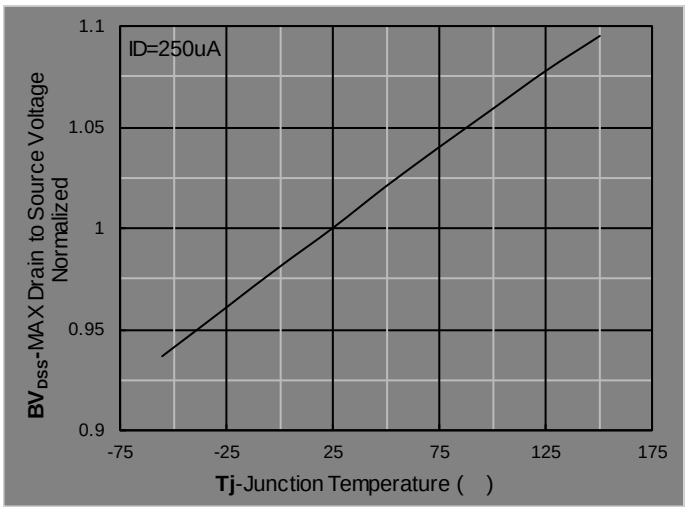


Figure 9. Normalized breakdown voltage

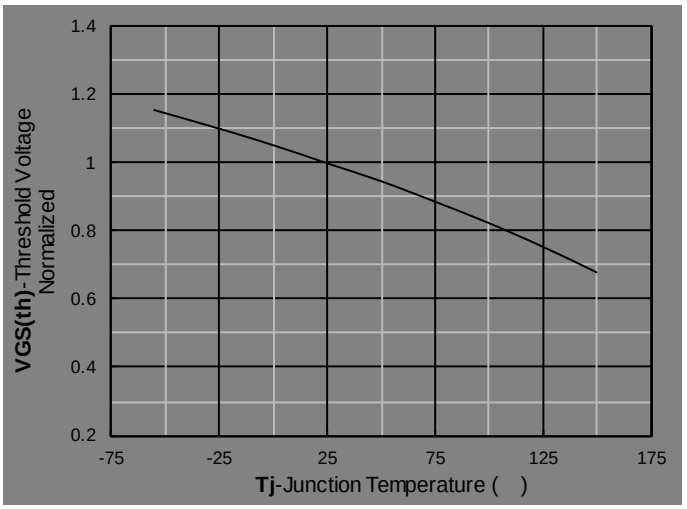


Figure 10. Normalized Threshold voltage

Figure 11. Current dissipation

Figure 12. Power dissipation

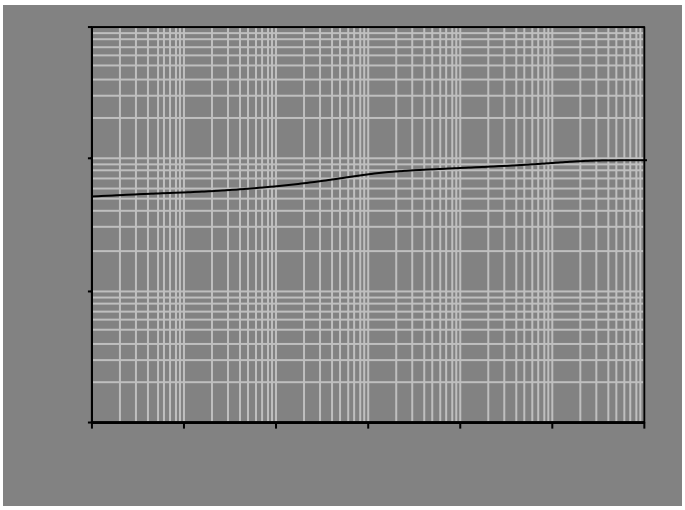
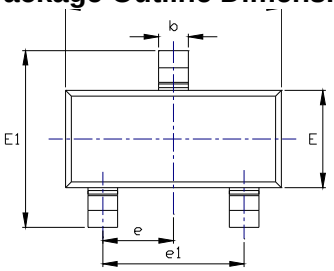


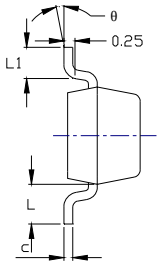
Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area

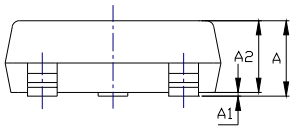
■ SOT-23 Package Outline Dimensions



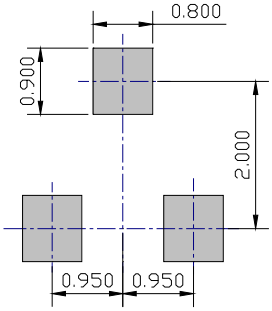
TOP VIEW



SIDE VIEW



SIDE VIEW



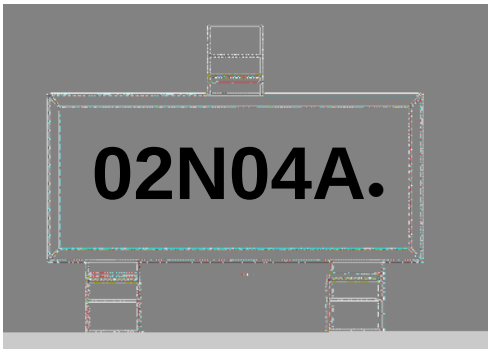
UNIT mm

SUGGESTED SOLDER PAD LAYOUT

DIMENSIONS				
SYMBOL	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

■ Marking Information



Note:
1. All marking is at middle of the product body
2. All marking is in laser marking
3. 02N04A is Marking Code
4. Body color: Black

Disclaimer

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