YJGD20G10A

RECOMMEND
YJGD20G10B
FOR NEW DESIGN

NMOS(Die1/Die2) Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= 20V, V_{DS}=0V			100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=15A		17	22	m
		V_{GS}= 4.5V, I_D=7A		21	27	
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.96	1.3	V
Maximum Body-Diode Continuous Current	I_S				20	A
Gate Resistance	R_g	f=1MHz		1.2		
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ		1051		pF
Output Capacitance	C_{oss}			399		
Reverse Transfer Capacitance	C_{rss}			18		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=10A		16		nC
Gate-Source Charge	Q_{gs}			5.6		
Gate-Drain Charge	Q_{gd}			2.4		
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=100A/us		42		
Reverse Recovery Time	t_{rr}			39.8		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V,I_D=4.0A R_{GEN}=3.0		39.2		
Turn-on Rise Time	t_r			11		
Turn-off Delay Time	$t_{D(off)}$			53.2		
Turn-off fall Time						

v NMOS(Die1/Die2)

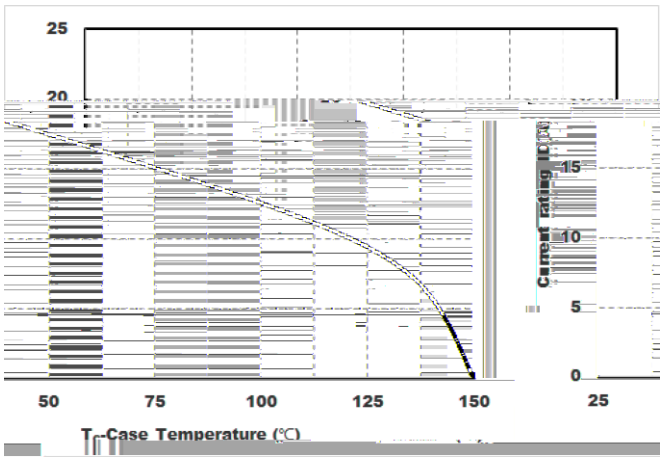


Figure7. Drain current

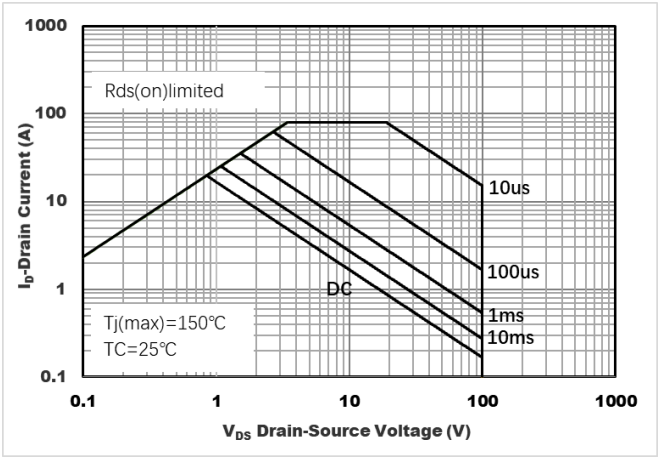


Figure8.Safe Operation Area

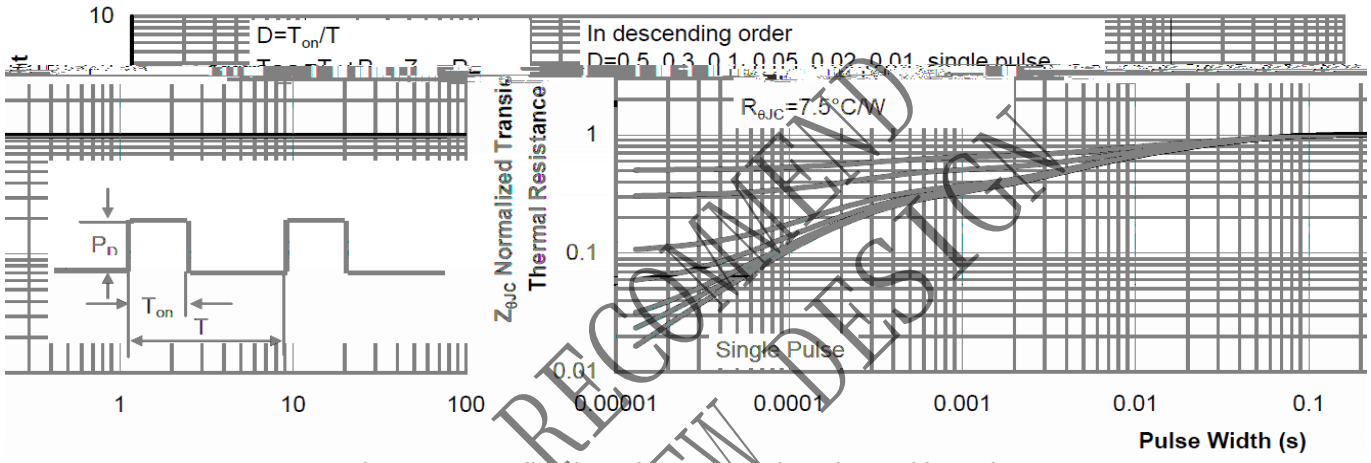
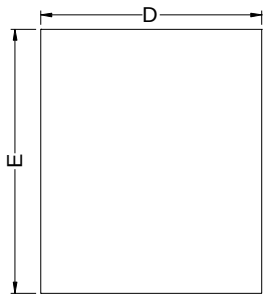


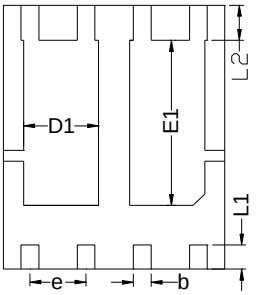
Figure9.Normalized Maximum Transient thermal impedance

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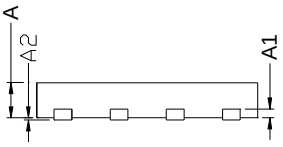
DFN5060-8L Package information



Top View



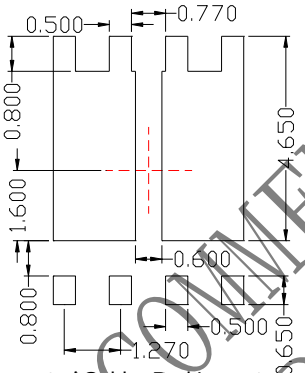
Bottom View



Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	4.90	5.00	5.10
E	5.90	6.00	6.10
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	1.60	1.70	1.80
E1	3.65	3.75	3.85
L1	0.45	0.55	0.65
L2		0.80 BSC	
b	0.30	0.40	0.50
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.10mm.
3.The pad layout is for reference purposes only.



Suggested Solder Pad Layout
Top View

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