N-Channel and N-Channel Complementary MOSFET

Product Summary

- V_{DS} 100V
- I_D 3A
- $R_{DS(ON)}$(at V_{GS}=10V) 260mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 270mΩ
- 100% EAS Tested

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Fast Switching Speed
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- DC-DC convertor

■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	1	A
	T_A=100℃		0.6	
	T_C=25℃		3	
	T_C =100℃		1.9	
Pulsed Drain Current [A]		I_{DM}	10	A
Avalanche energy [B]		EAS	4	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	1.6	W
	T_A=100℃		0.6	
	T_C=25℃		14.7	
	T_C =100℃		5.8	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	℃

■Thermal resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [C]				

■ **Electrical Characteristics** (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=150℃	-	-	100	

Typical Electrical and Thermal Characteristics Diagrams

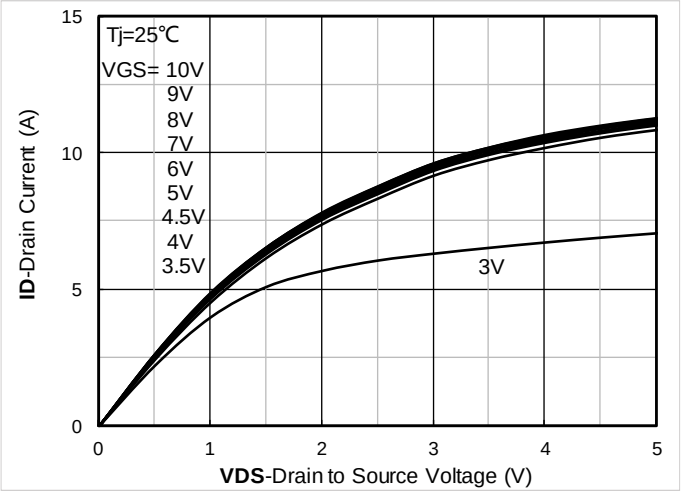


Figure 1. Output Characteristics

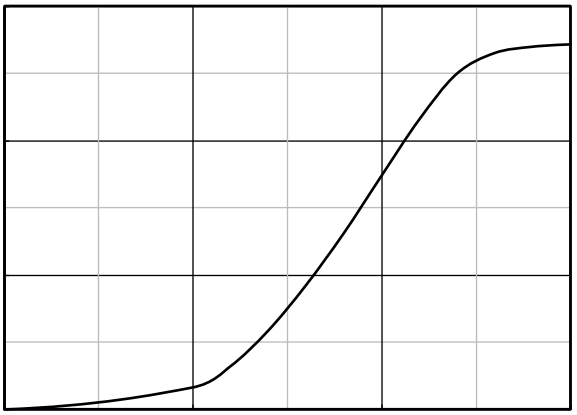


Figure 2. Transfer Characteristics

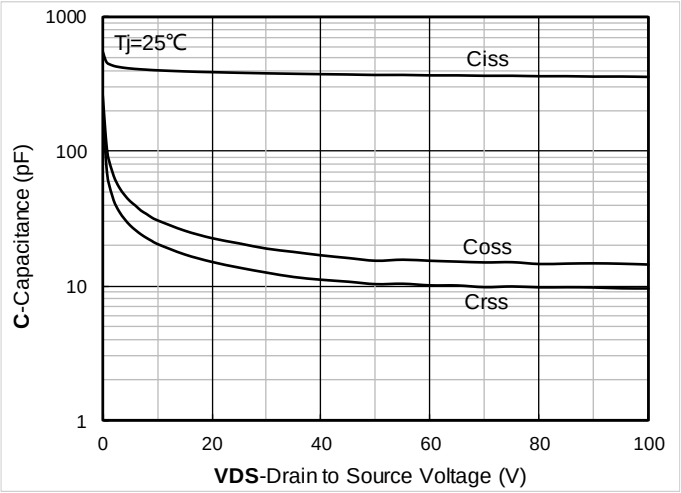


Figure 3. Capacitance Characteristics

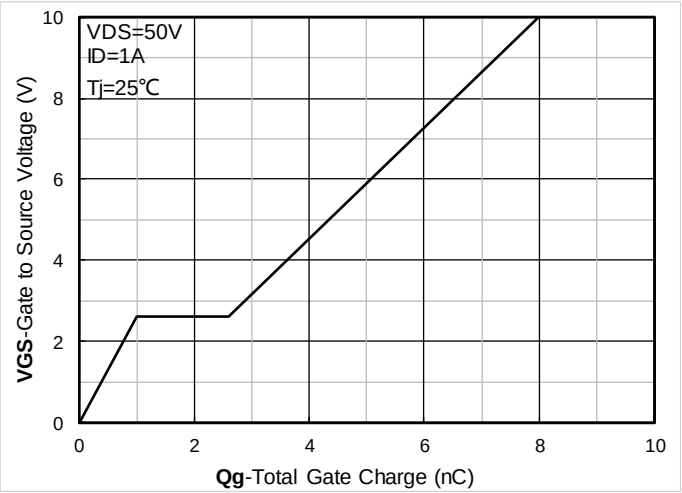


Figure 4. Gate Charge

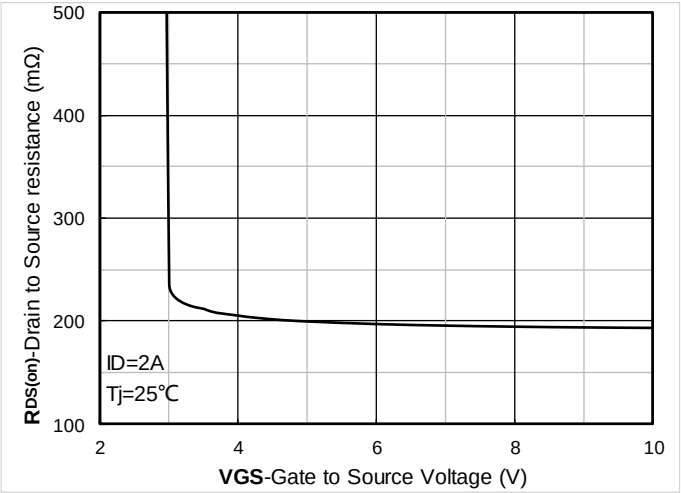


Figure 5. On-Resistance vs Gate to Source Voltage

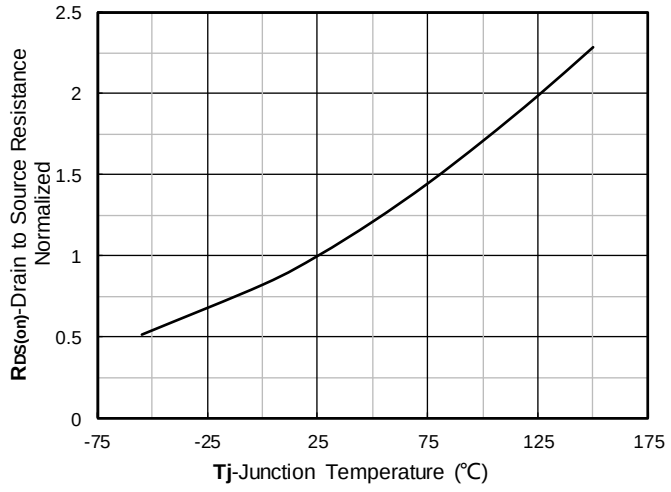


Figure 6. Normalized On-Resistance

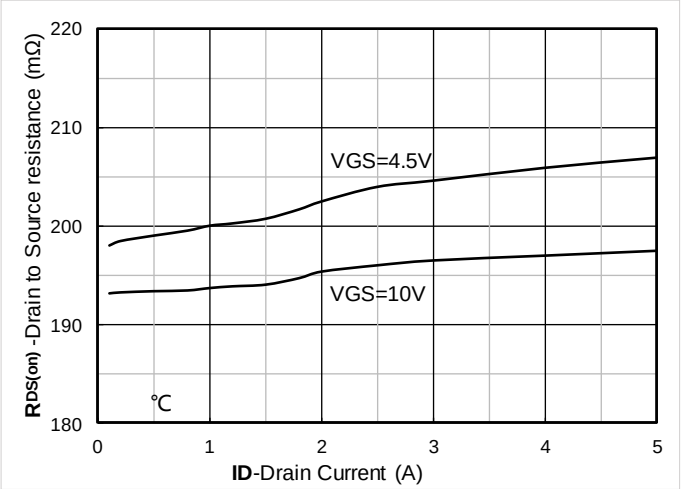


Figure 7. $R_{DS(on)}$ VS Drain Current

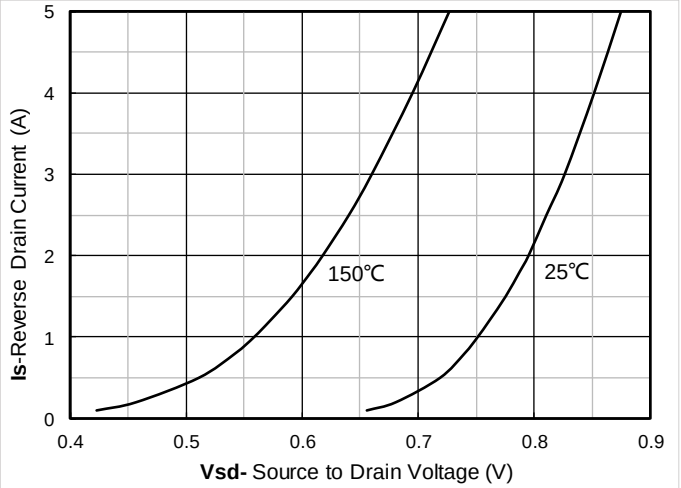


Figure 8. Forward characteristics of reverse diode

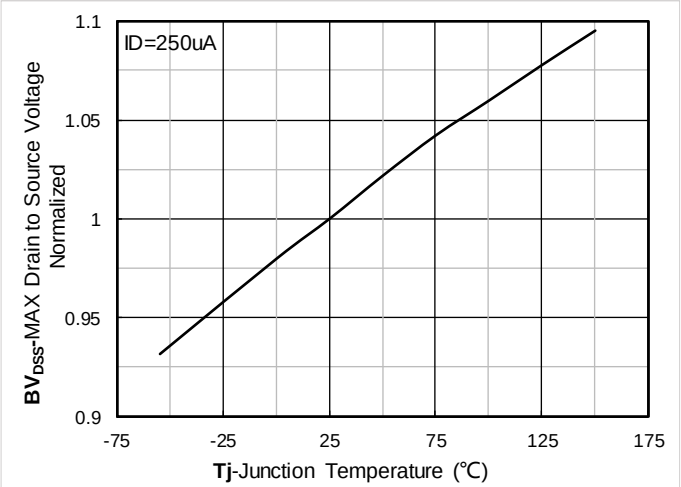


Figure 9. Normalized breakdown voltage

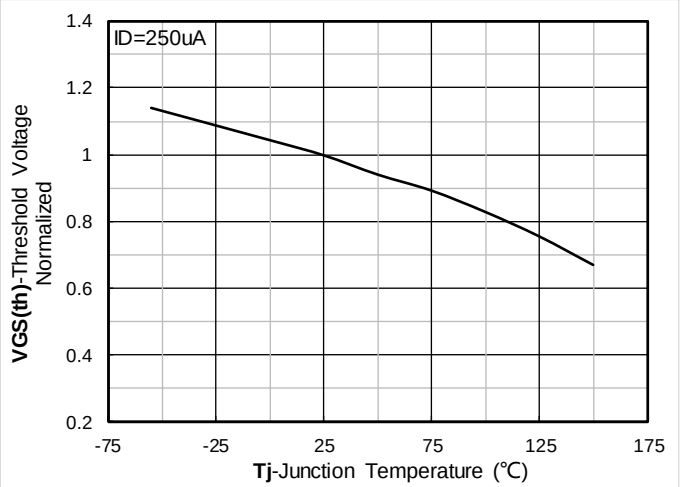


Figure 10. Normalized Threshold voltage

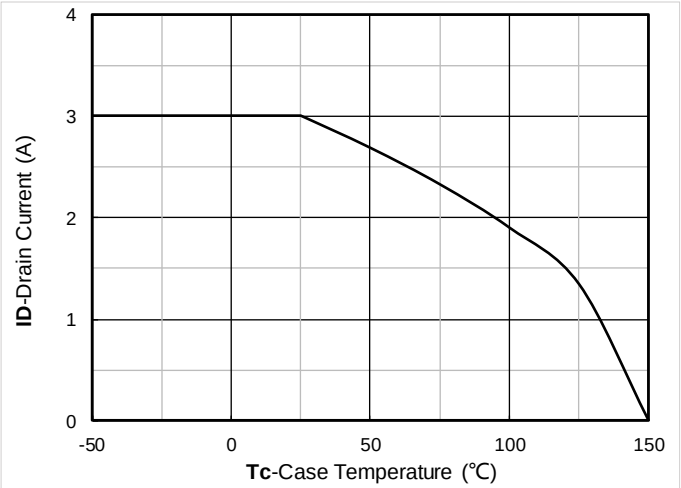


Figure 11. Current dissipation

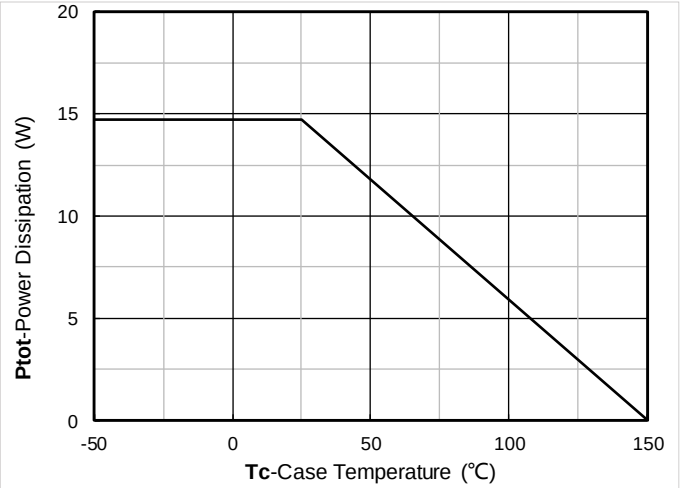


Figure 12. Power dissipation

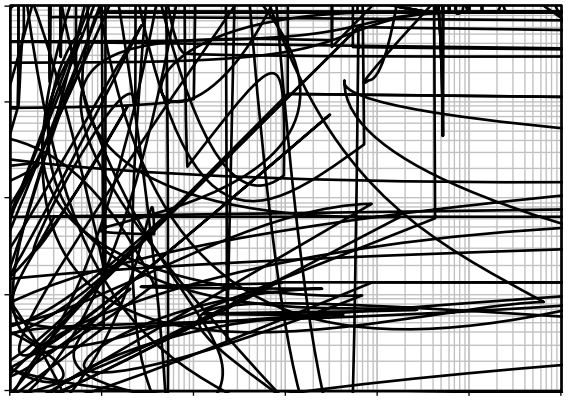


Figure 13. Maximum Transient Thermal Impedance

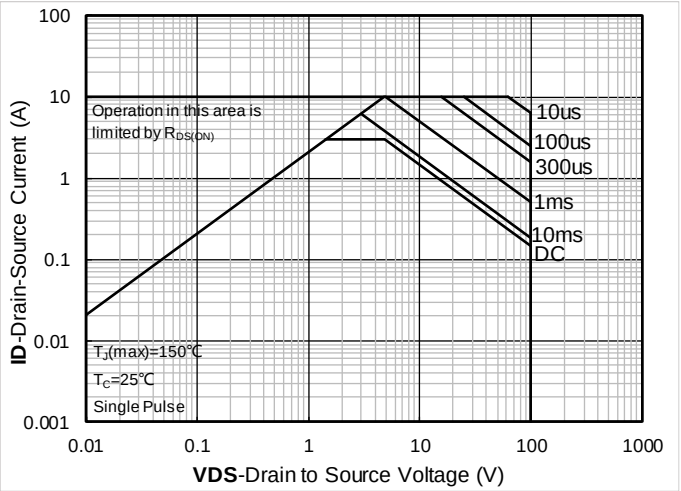


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

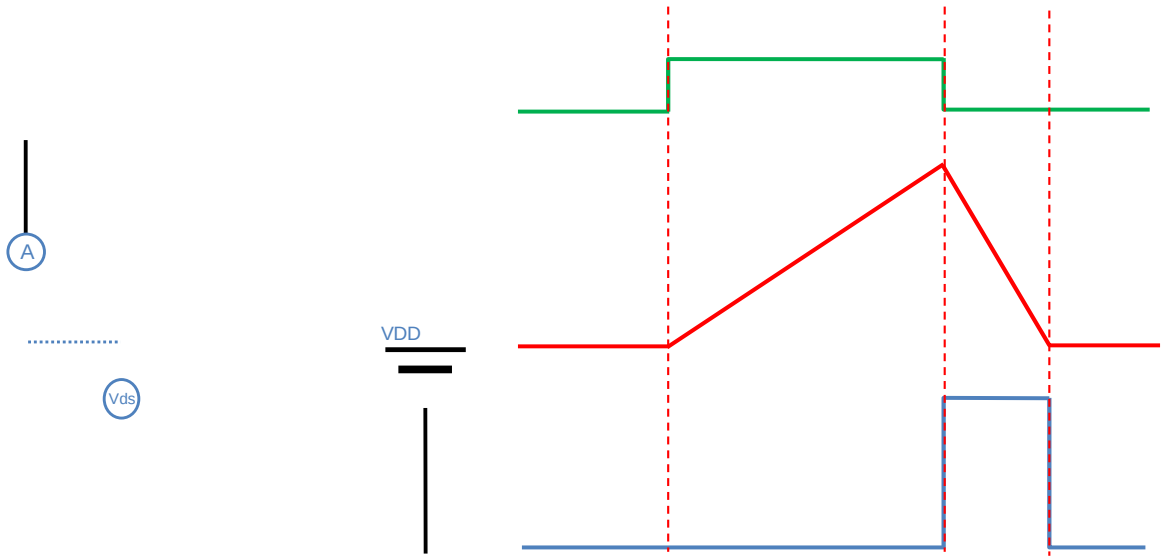


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

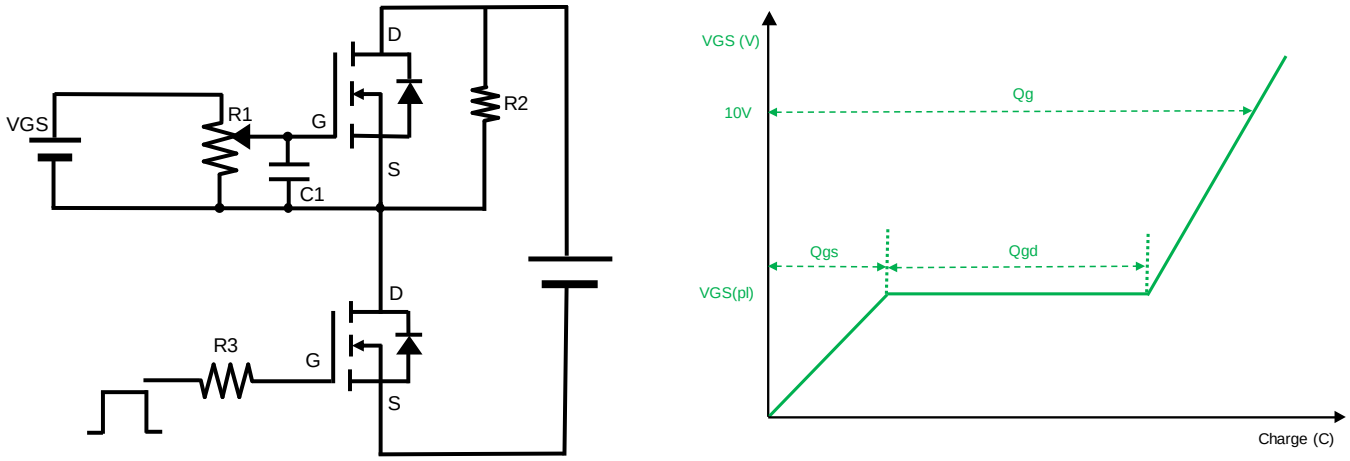


Figure B. Gate Charge Test Circuit & Waveform

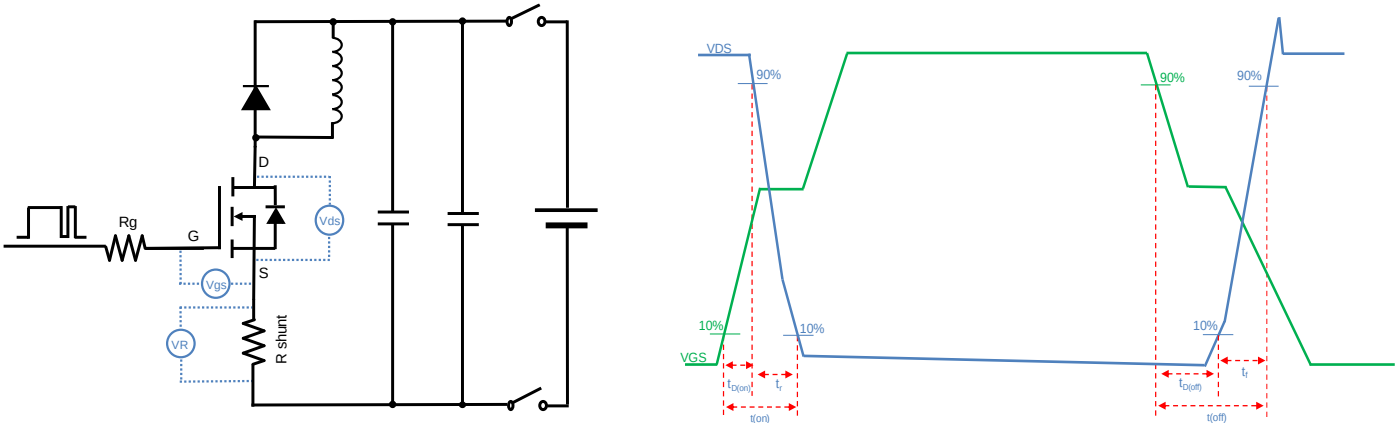


Figure C. Resistive Switching Test Circuit & Waveform

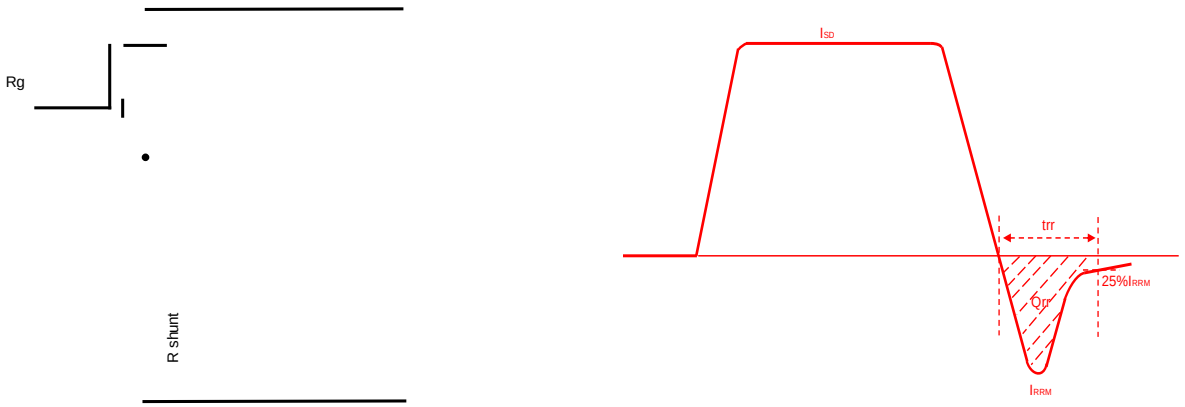


Figure D. Diode Recovery Test Circuit & Waveform

■ DFN5060-8L Package information

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	4.90	5.0	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.10mm.
3.The pad layout is for reference purposes only.

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