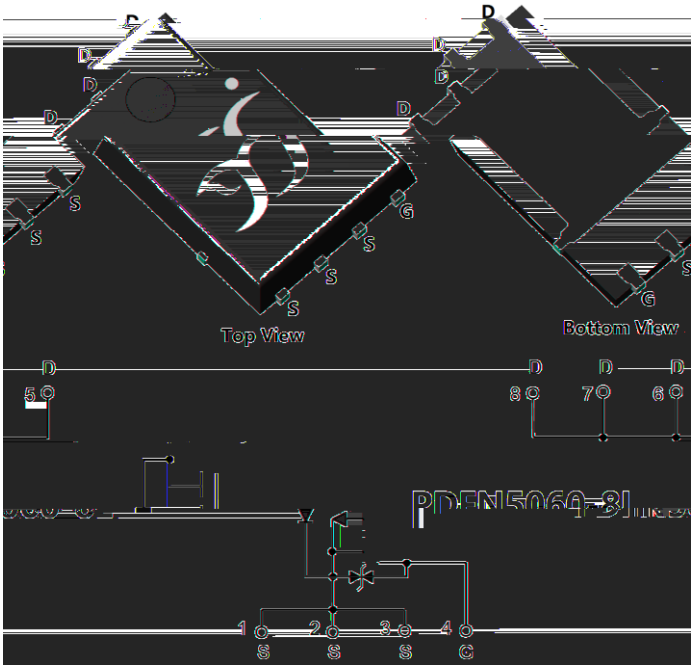
P-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	-60V
I_D	-46A
$R_{DS(ON)}$(at V_{GS}=-10V)	27m
100% EAS Tested	
100% V_{DS} Tested	
ESD Level(HBM)	Class 3A

General Description

Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free
-Q101 qualified

Applications

Power management functions
Synchronous-rectification application
DC-DC convertor

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	-60	V
Gate-source Voltage (Note 4)			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25℃,V_{GS}=-10V	I_D	-	-6.7	A
		T_A=100℃,V_{GS}=-10V		-	-4.7	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25℃,V_{GS}=-10V,Chip limitation		-	-46	
		T_C=100℃,V_{GS}=-10V		-	-32	
Pulsed Drain Current	T_C=25 ,t_p≤10μs		I_{DM}	-	-160	
Maximum Body-Diode Continuous Current	T_C=25		I_S		-46	
Avalanche Energy (non-repetitive)	T_J=25℃,V_G=-10V,R_G L=0.5mH,I_{AS}=-21A		EAS	-	110.25	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25℃	P_D	-	2.6	W
		T_A=100℃		-	1.3	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25℃		-	125	
		T_C=100℃		-	62.5	
Junction and Storage Temperature Range			T_J ,T_{STG}	-55	175	℃

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	R	-	56	℃/W
Thermal Resistance Junction-to-Case	Steady-State	R	-	1.2	

Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG027P06AKHQ	F1	YJG027P06AK	5000	10000	100000	

Electrical Characteristics

Parameter	Symbol

Typical Electrical and Thermal Characteristics Diagrams

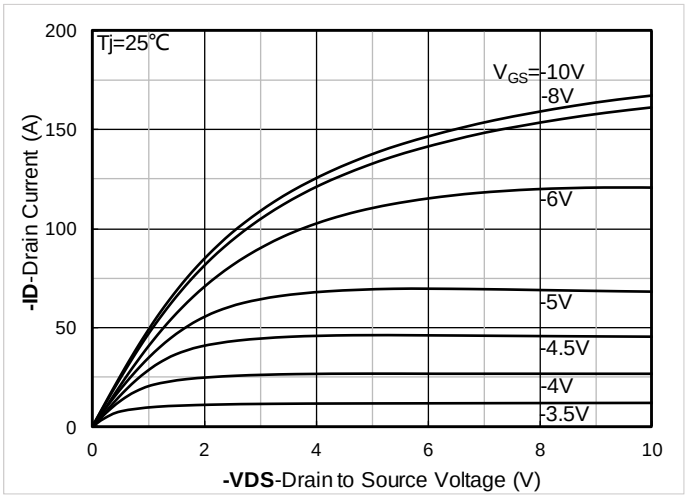


Figure 1. Output Characteristics; typical values

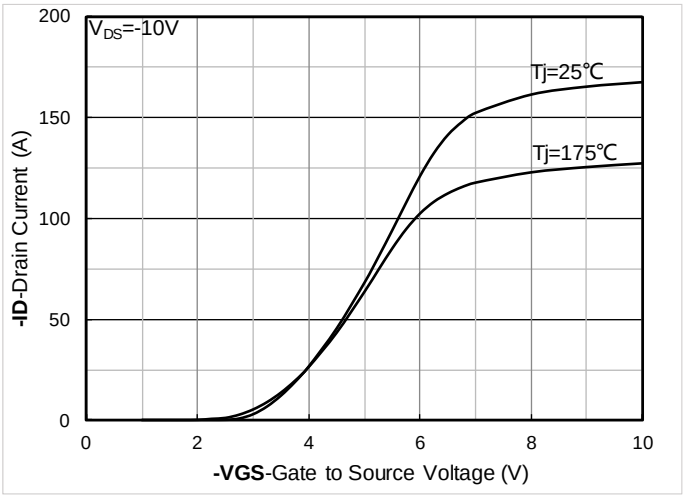


Figure 2. Transfer Characteristics; typical values

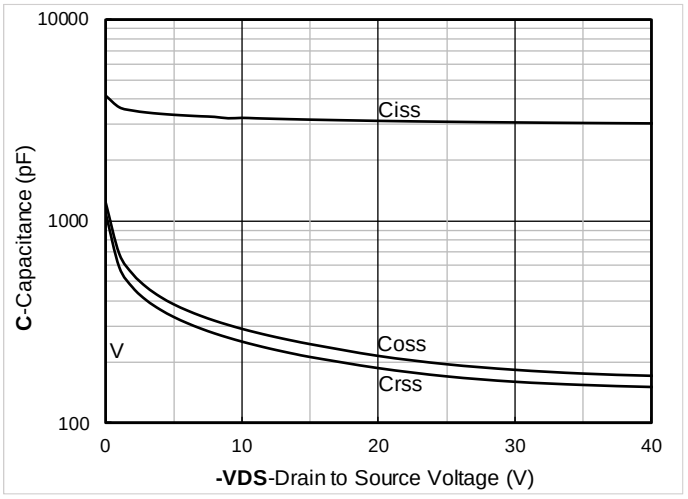


Figure 3. Capacitance Characteristics; typical values

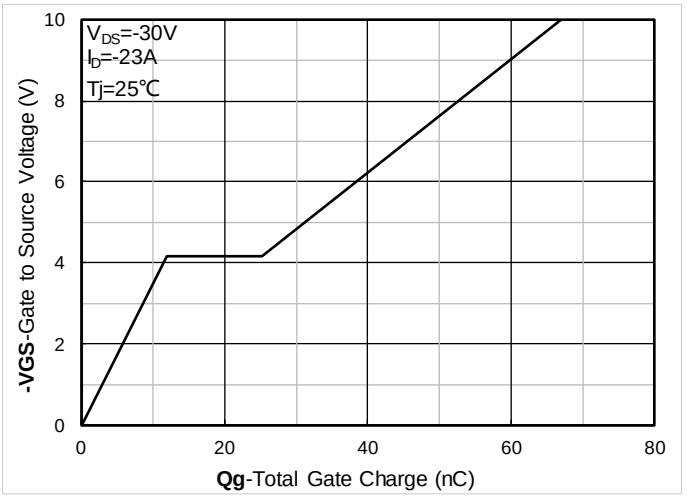


Figure 4. Gate Charge; typical values

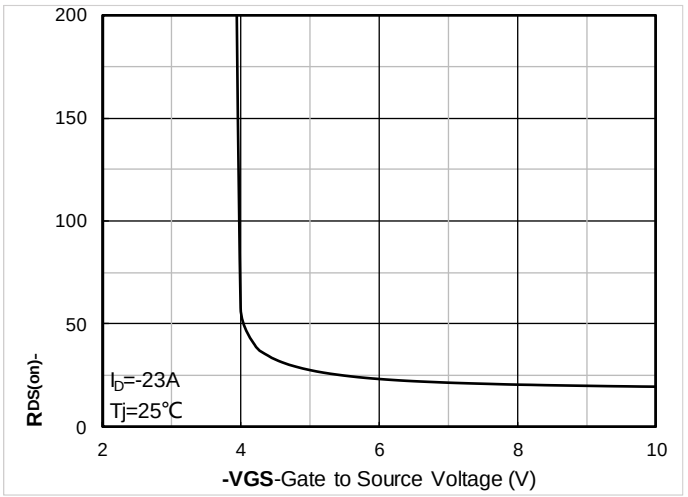


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

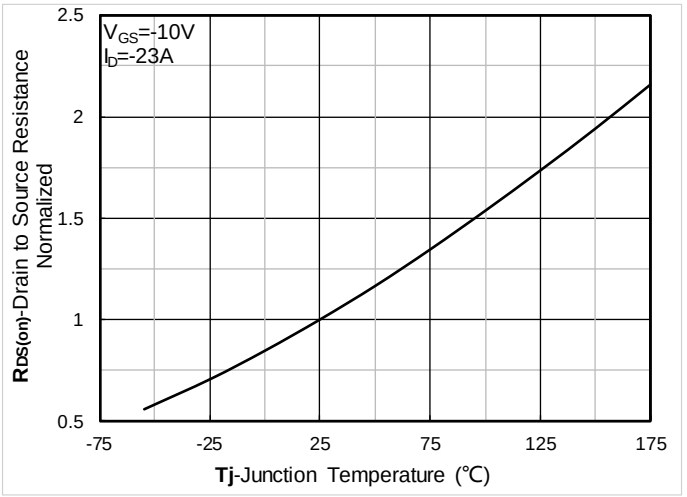


Figure 6. Normalized On-Resistance

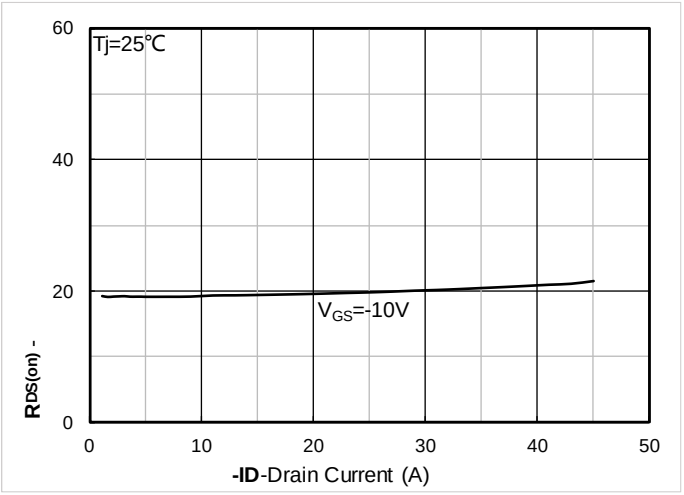


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

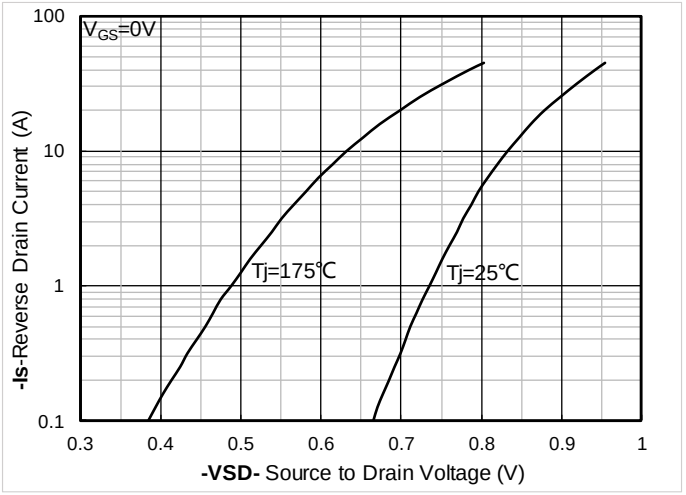


Figure 8. Forward characteristics of reverse diode; typical values

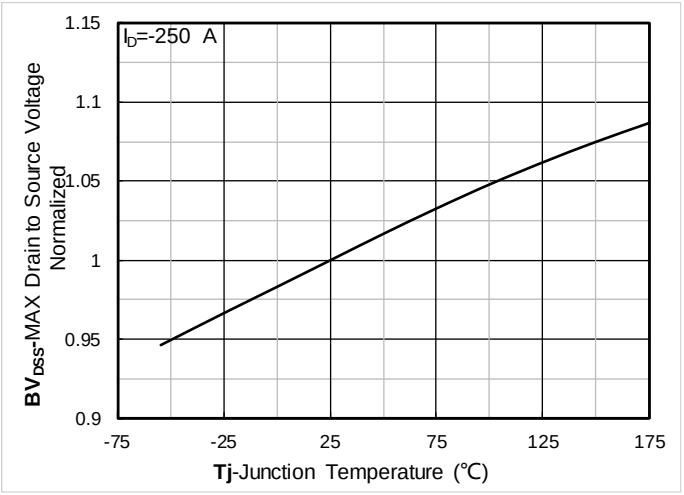


Figure 9. Normalized breakdown voltage

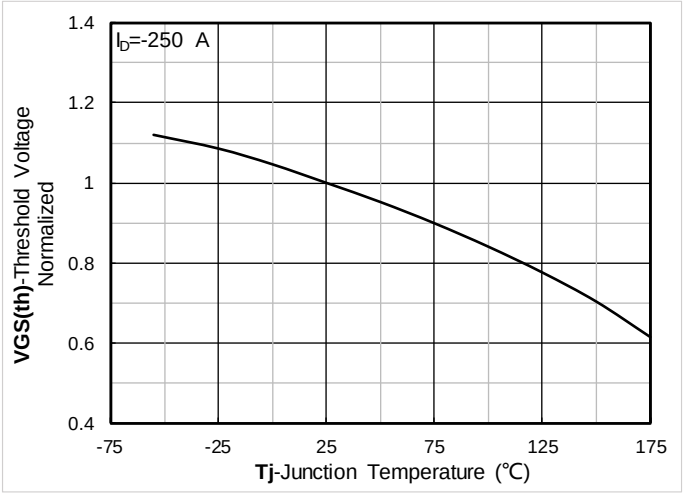


Figure 10. Normalized Threshold voltage

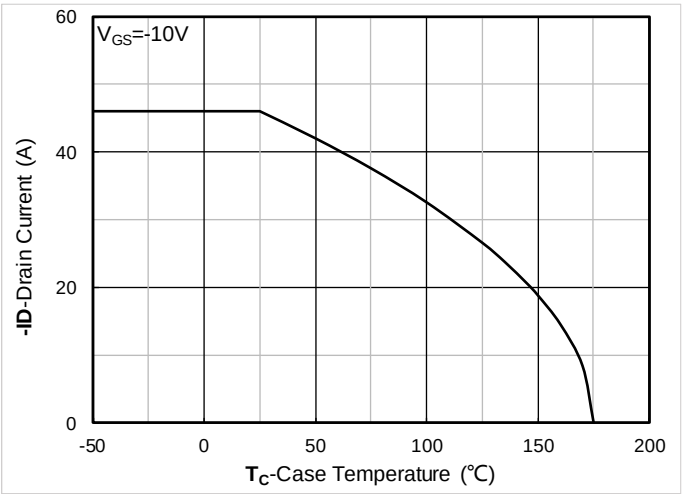


Figure 11. Current dissipation

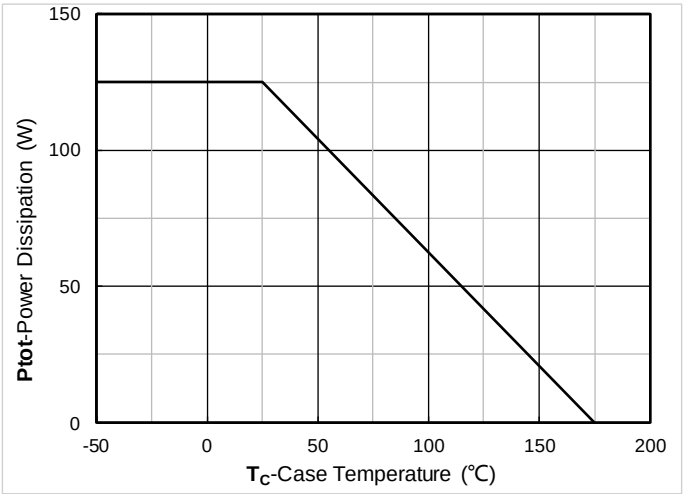


Figure 12. Power dissipation

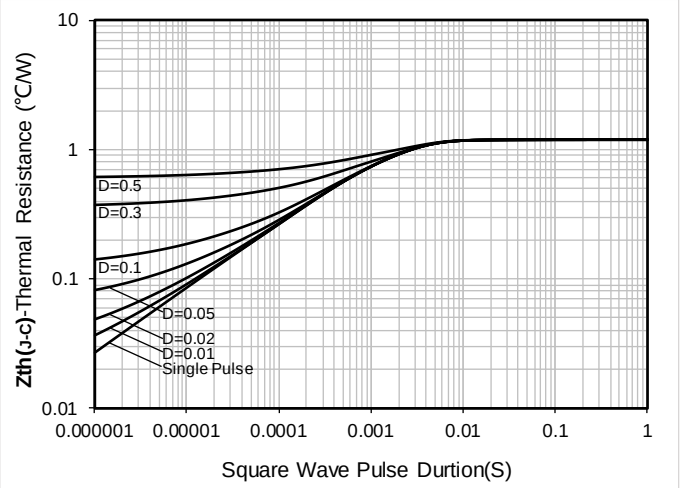


Figure 13. Maximum Transient Thermal Impedance

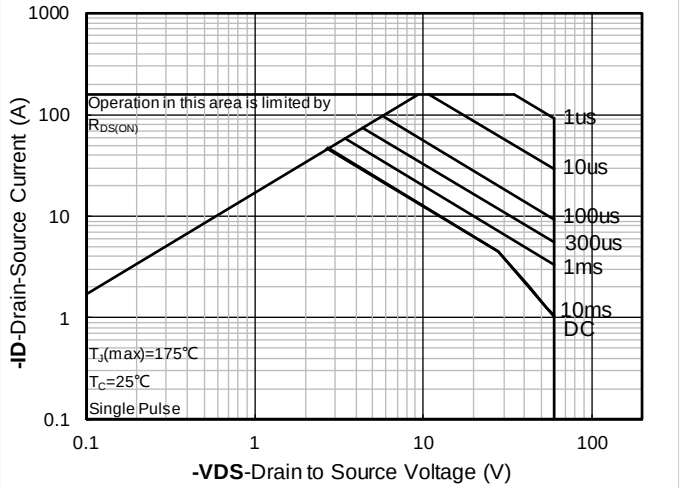
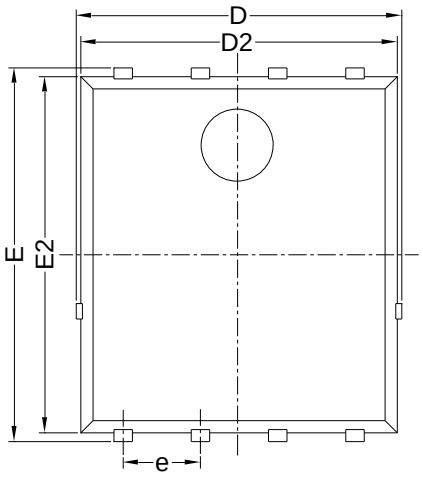
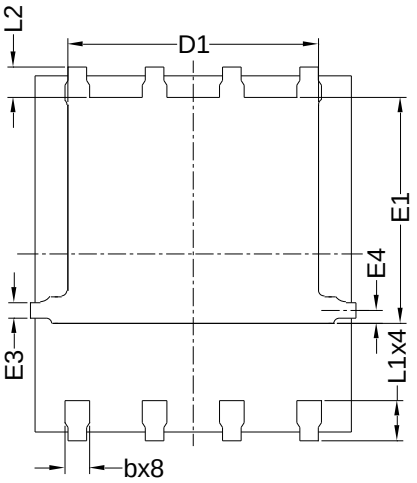


Figure 14. Safe Operation Area

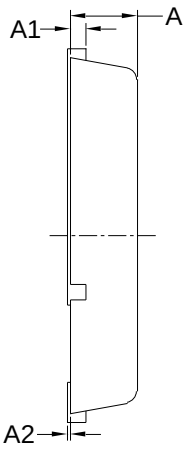
PDFN5060-8L-B-1.1MM Package information



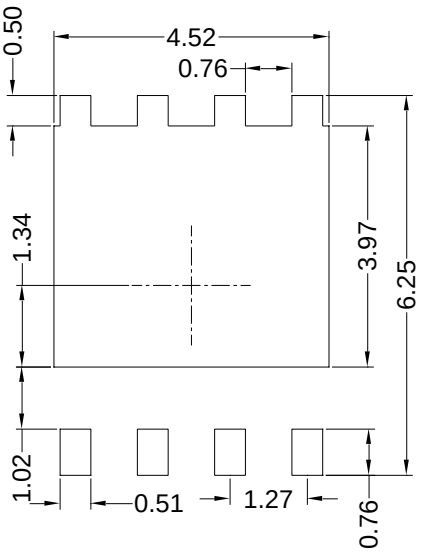
Top View



Bottom View



Side View

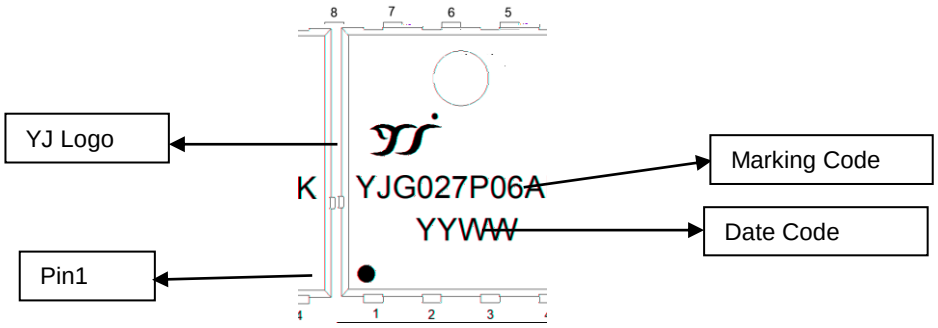


Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

Marking Information



Note
1. All marking is at middle of the product body
2. All marking is in laser printing
3. YJG027P06AK is marking code, YYWW is date code,
4. Body color: Black

Disclaimer

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