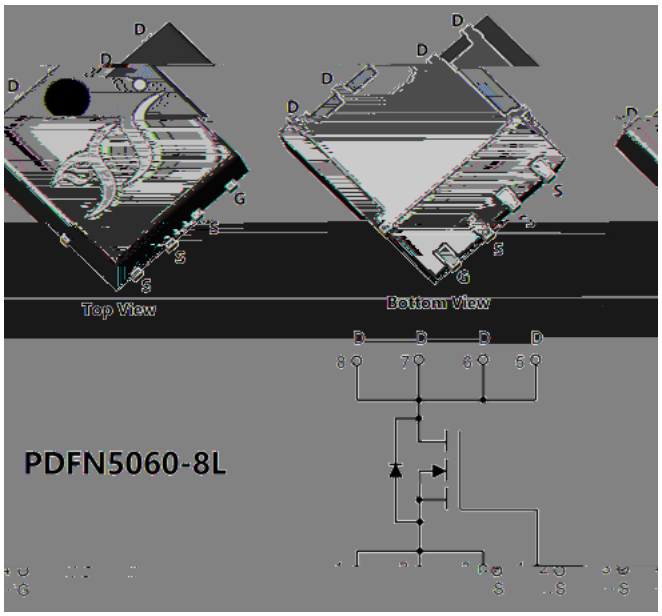
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 100V
- I_D 40A
- $R_{DS(ON)}$(at V_{GS}=10V) 17mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 22mΩ
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- 12V,24V and 48V Automotive systems

■ Absolute Maximum Ratings (T_J=25 unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	100	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25	I_D	8.5	A
		T_A=100		6	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25		40	
		T_C =100		28	
Pulsed Drain Current	T_C=25 , t =100μs		I_{DM}	150	A
Avalanche energy	V_G=10V, R_G=25Ω, L=0.5mH, IAS=16A		EAS	64	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25	P_D	2.7	W
		T_A=100		1.3	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25		71	
		T_C =100		35	
Junction and Storage Temperature Range			T_J , T_{STG}	-55 +175	

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	46	55	/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.7	2.1	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG017G10AHQ	F1	YJG017G10A	5000	10000	100000	13" reel

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=125	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.3	1.8	2.3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	13	17	mΩ
		V_{GS}=4.5V, I_D=20A	-	16	22	
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	1.2	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	40	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	1170	-	pF
Output Capacitance	C_{oss}		-	340	-	
Reverse Transfer Capacitance	C_{rss}		-	12	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=50V, I_D=20A	-	19.8	-	nC
Gate-Source Charge	Q_{gs}		-	2.2	-	
Gate-Drain Charge	Q_{gd}		-	2	-	
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=100A/us	-	41.3	-	nC
Reverse Recovery Time	t_{rr}		-	37.1	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=50V, I_D=20A R_{GEN}=2.7Ω	-	10.2	-	ns
Turn-on Rise Time	t_r		-	3.6	-	
Turn-off Delay Time	$t_{D(off)}$		-	22.9	-	
Turn-off fall Time	t_f		-	4.6	-	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FЙ $ f ! i4h m T ъ ' ≠

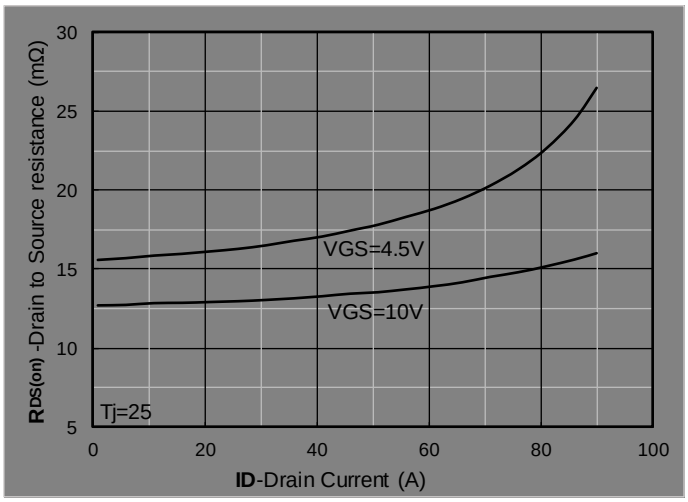


Figure 7. $R_{DS(on)}$ VS Drain Current

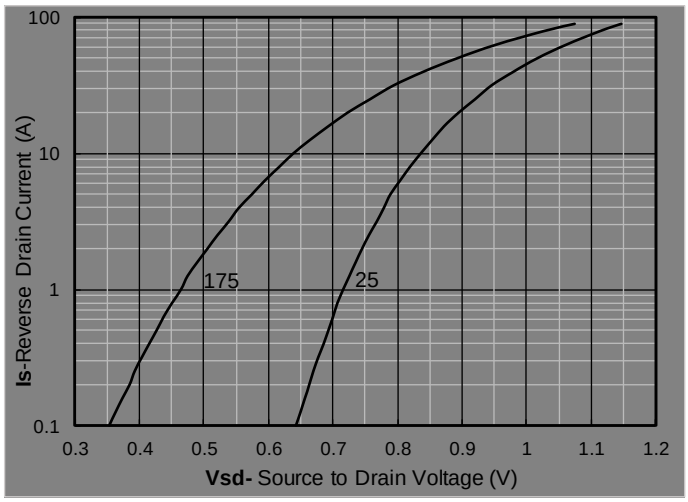


Figure 8. Forward characteristics of reverse diode

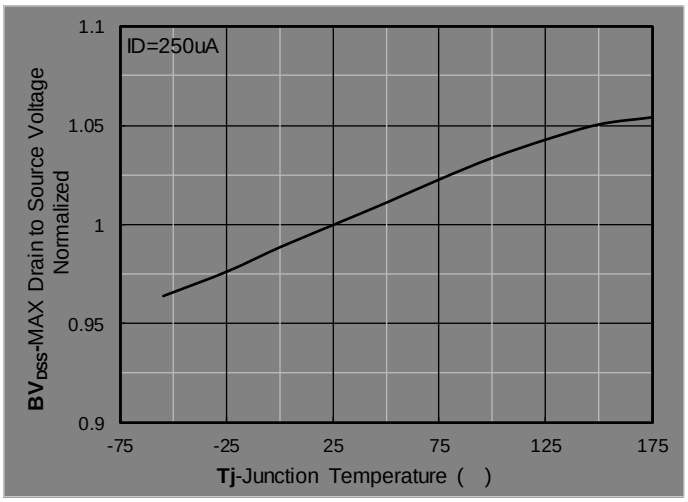


Figure 9. Normalized breakdown voltage

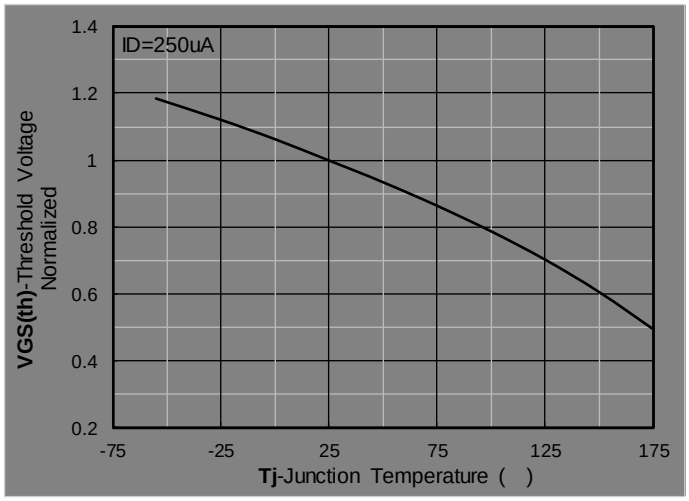


Figure 10. Normalized Threshold voltage

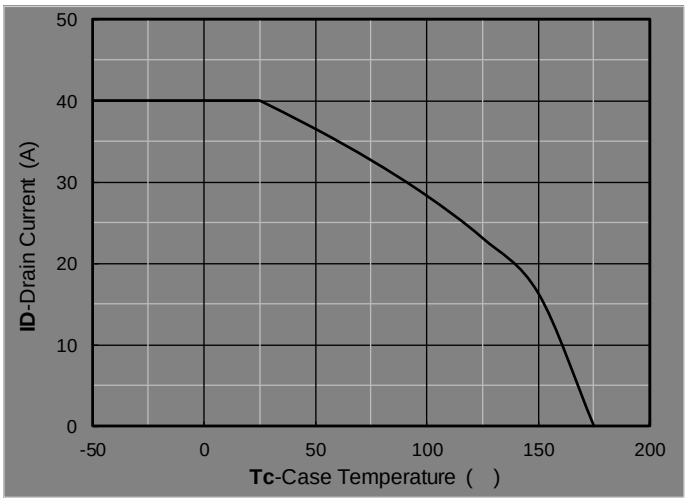


Figure 11. Current dissipation

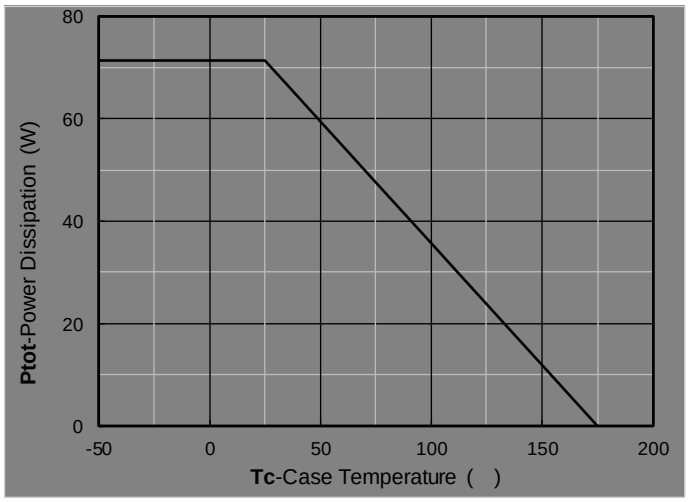
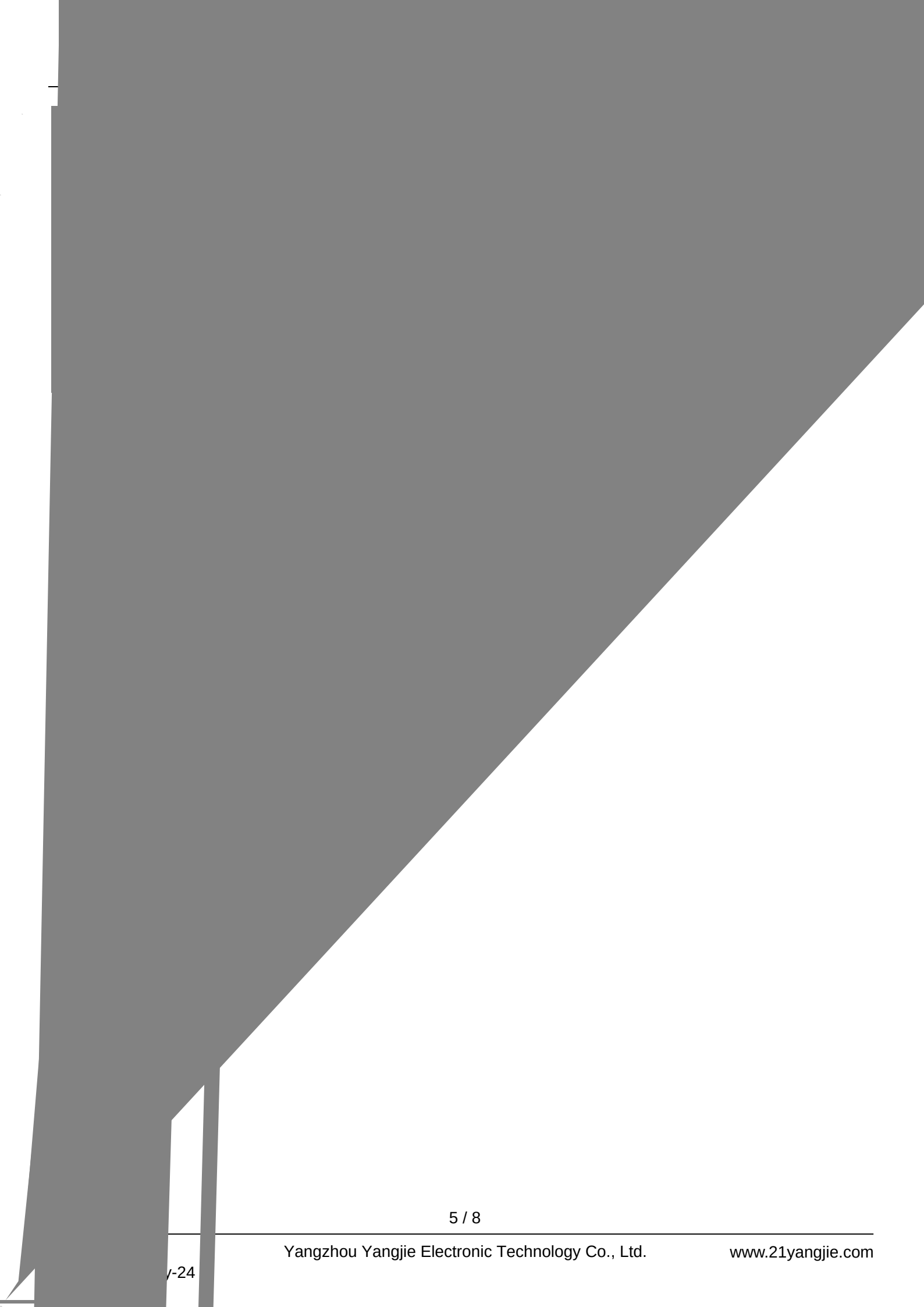


Figure 12. Power dissipation



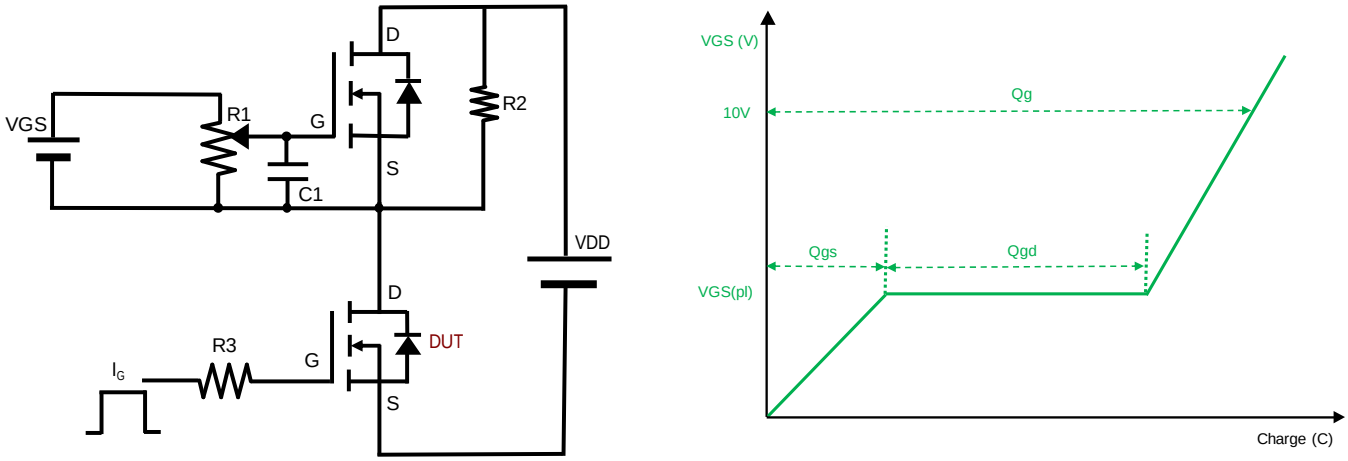


Figure B. Gate Charge Test Circuit & Waveform

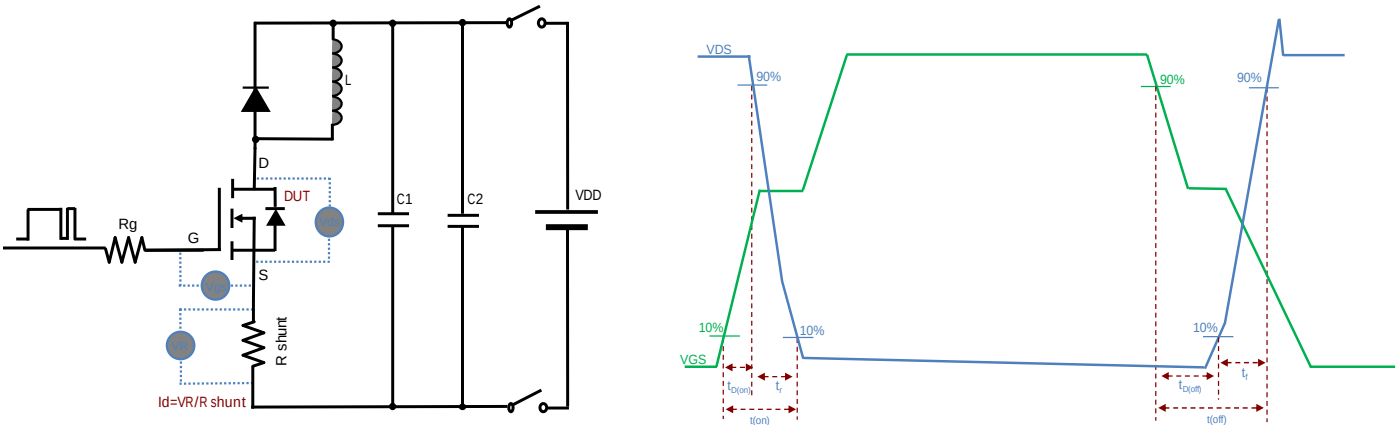


Figure C. Resistive Switching Test Circuit & Waveform

■ PDFN5060-8L-B-1.1MM Package information

Note:

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