N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	60V
I_D	60A
$R_{DS(ON)}$(at V_{GS}=10V)	11m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Trench Power LV MOSFET technology
High density cell design for low RDS(ON)
Excellent stability and uniformity
1
-0 Flammability Rating
alogen Free

Applications

Power management
Portable equipment

Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	9	A
	T_A=100℃		5.7	
	T_C=25℃		60	
	T_C =100℃		37	
Pulsed Drain Current [A]		I_{DM}	180	A
Avalanche energy [B]		EAS	225	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	2.2	W
	T_A=100℃		0.9	
	T_C=25℃		73	
	T_C =100℃		29	

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250uA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V	-	-	1	
		V_{DS}=60V, V_{GS}=0V, Tj=150℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D	2	3	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A	-	8.2	11	
Diode Forward Voltage	V_{SD}	I_S=30A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	1.3	-	
Maximum Body-Diode Continuous Current	I_S		-	-	60	A
Dynamic Parameters						
Input Capacitance	C_{iss}		-	1935	-	
Output Capacitance	C	V_{DS}=30V, V_{GS}=0V, f=1MHz				pF

Typical Electrical and Thermal Characteristics Diagrams

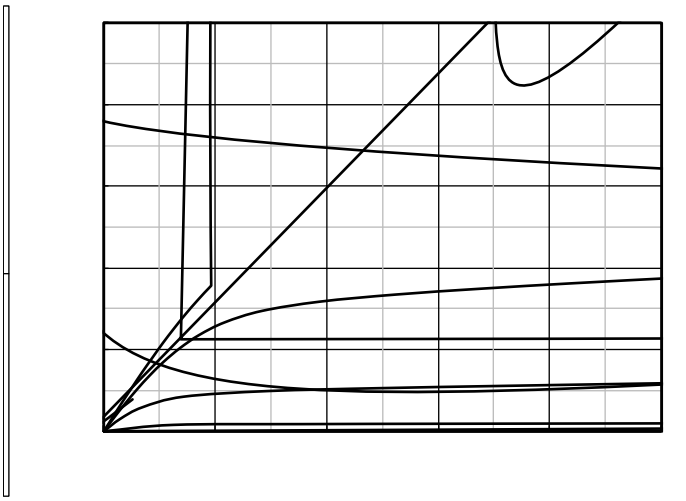


Figure 1. Output Characteristics

Figure 2. Transfer Characteristics

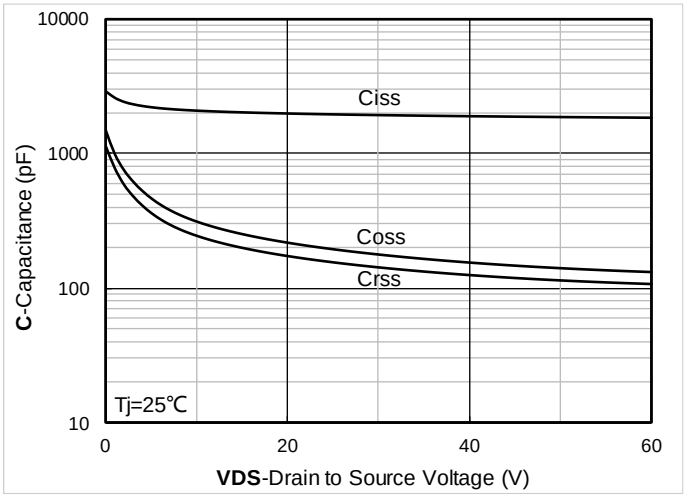


Figure 3. Capacitance Characteristics

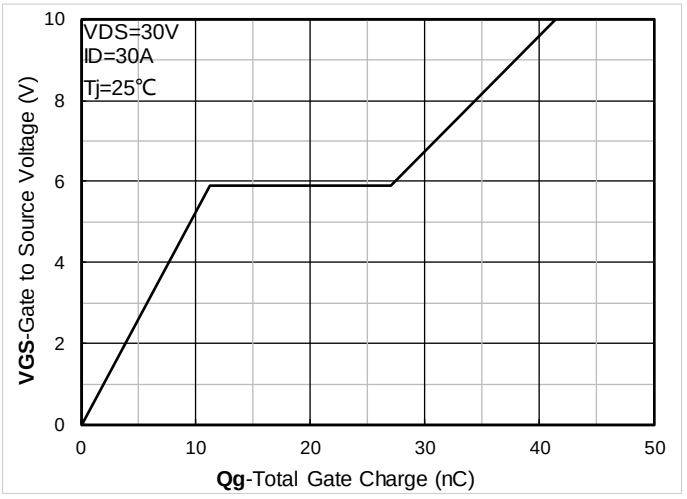


Figure 4. Gate Charge

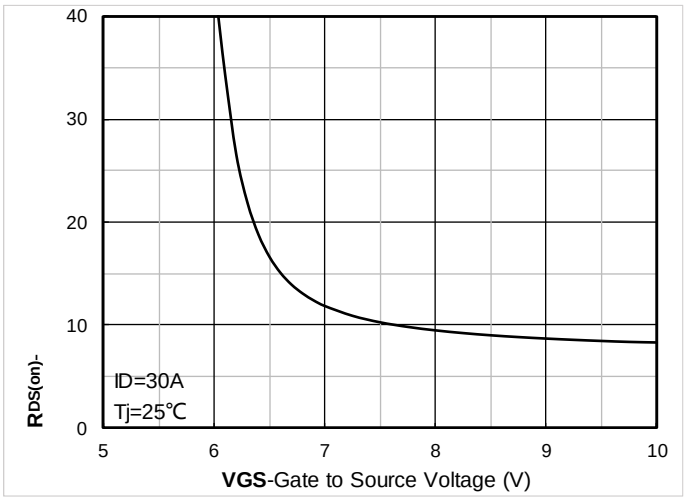


Figure 5. On-Resistance vs Gate to Source Voltage

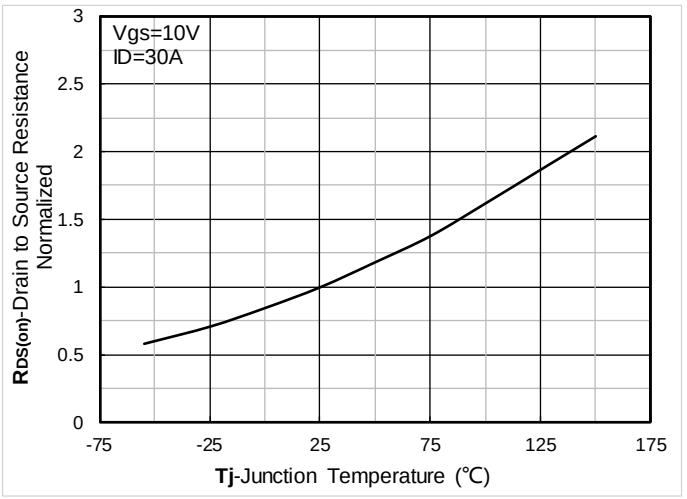


Figure 6. Normalized On-Resistance

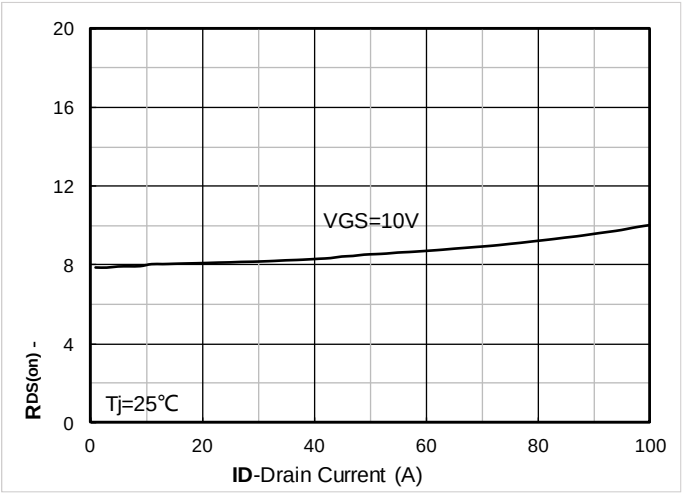


Figure 7. $R_{DS(on)}$ VS Drain Current

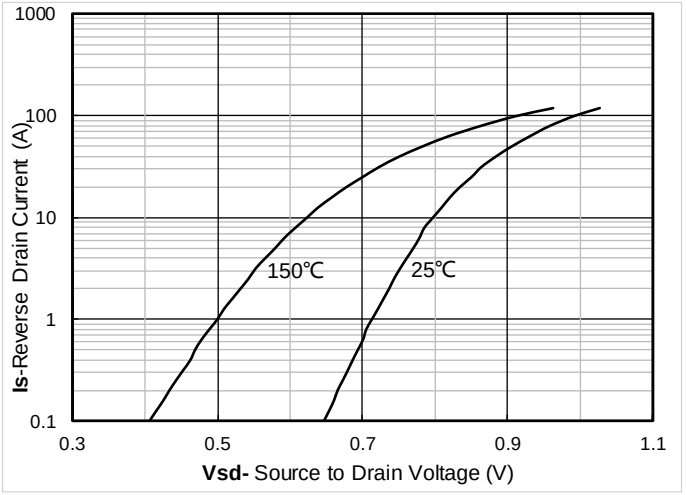


Figure 8. Forward characteristics of reverse diode

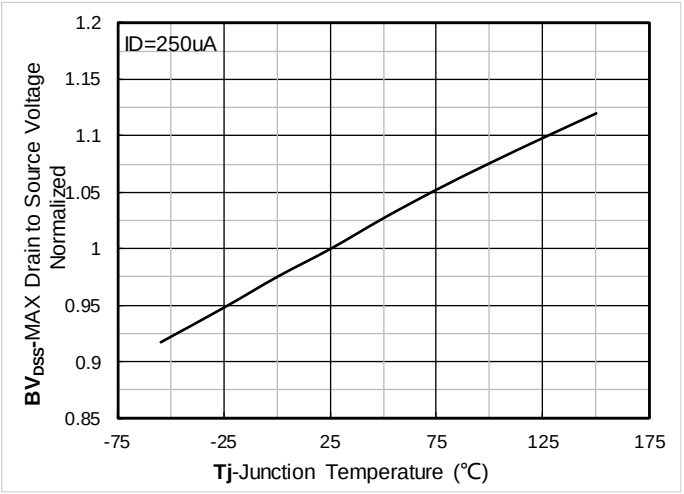


Figure 9. Normalized breakdown voltage

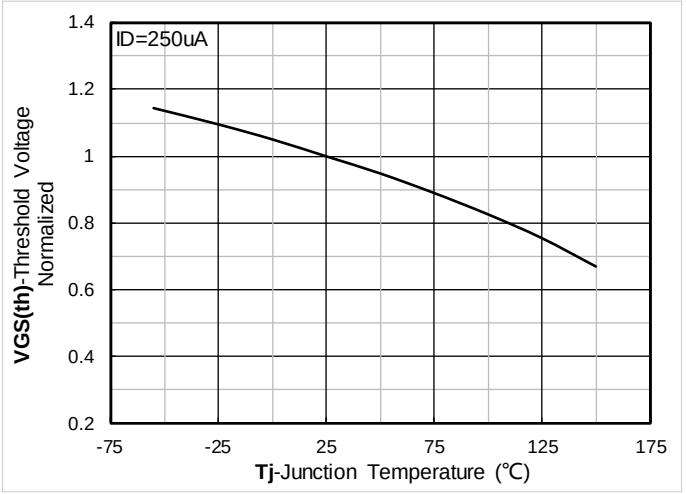


Figure 10. Normalized Threshold voltage

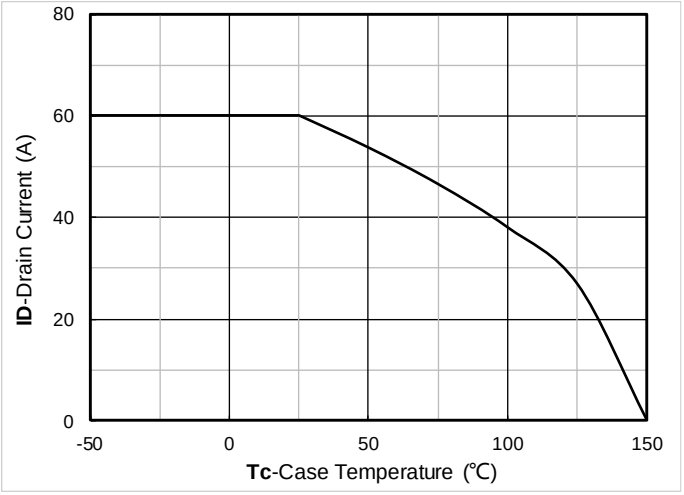


Figure 11. Current dissipation

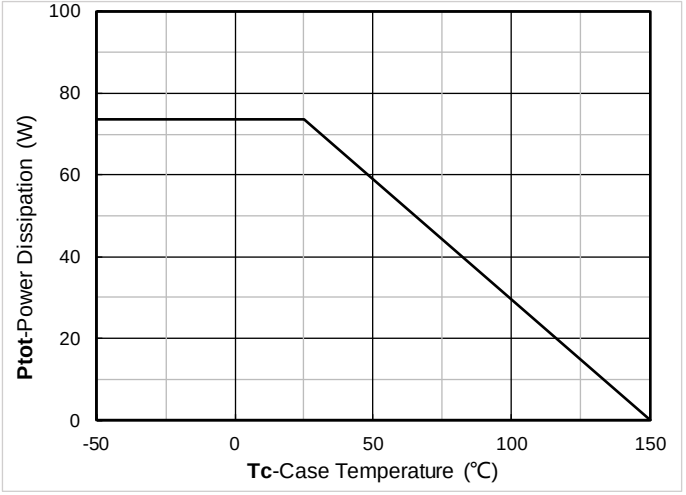


Figure 12. Power dissipation

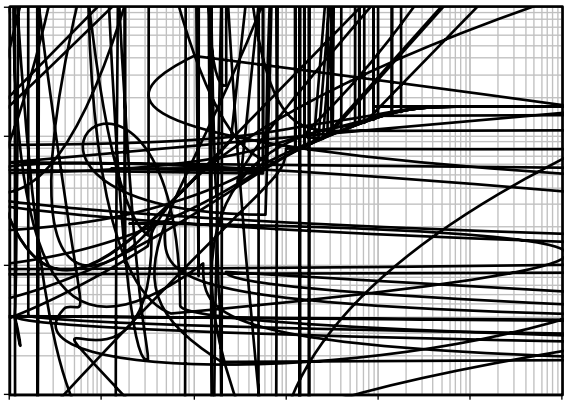


Figure 13. Maximum Transient Thermal Impedance

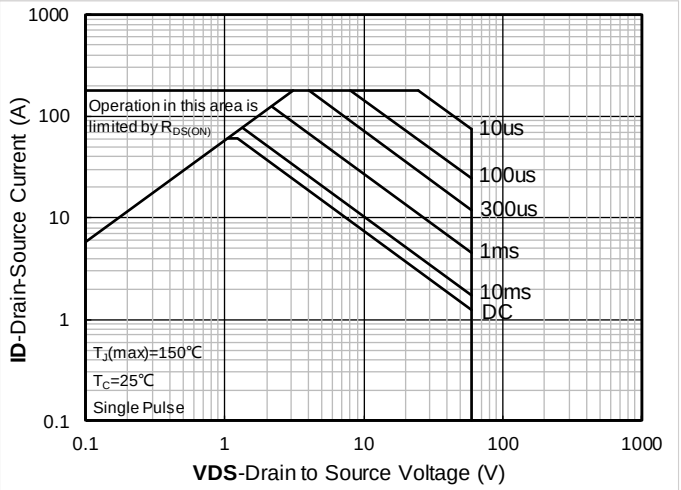


Figure 14. Safe Operation Area

Test Circuits & Waveforms

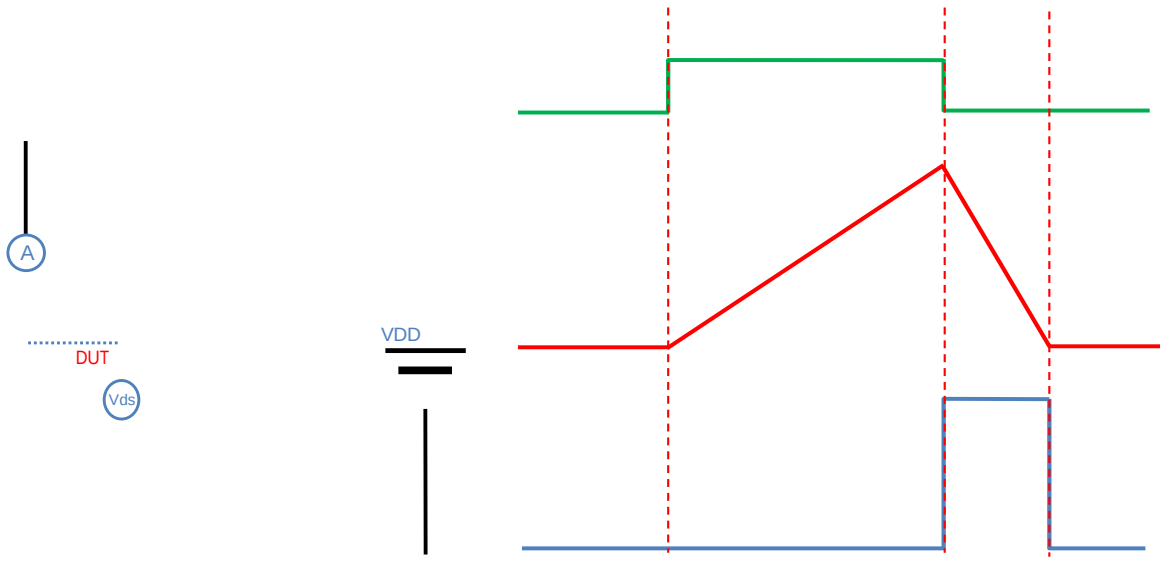


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

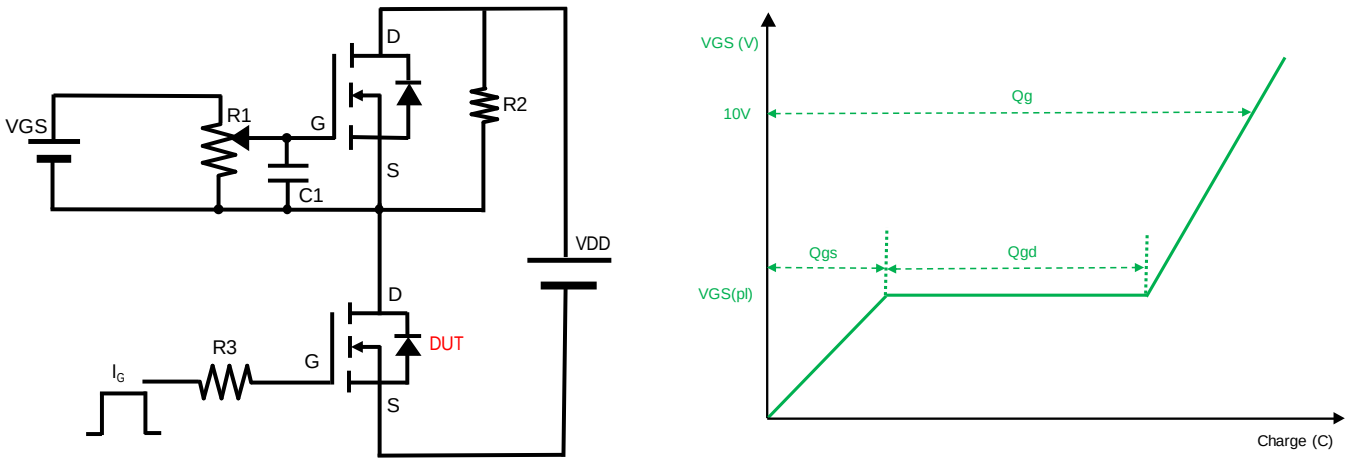


Figure B. Gate Charge Test Circuit & Waveform

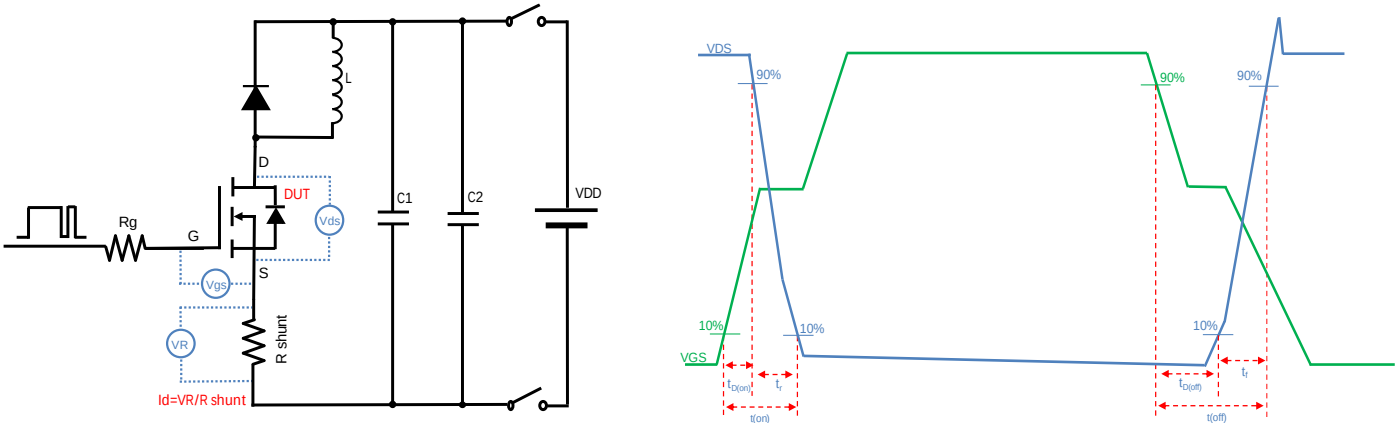


Figure C. Resistive Switching Test Circuit & Waveform

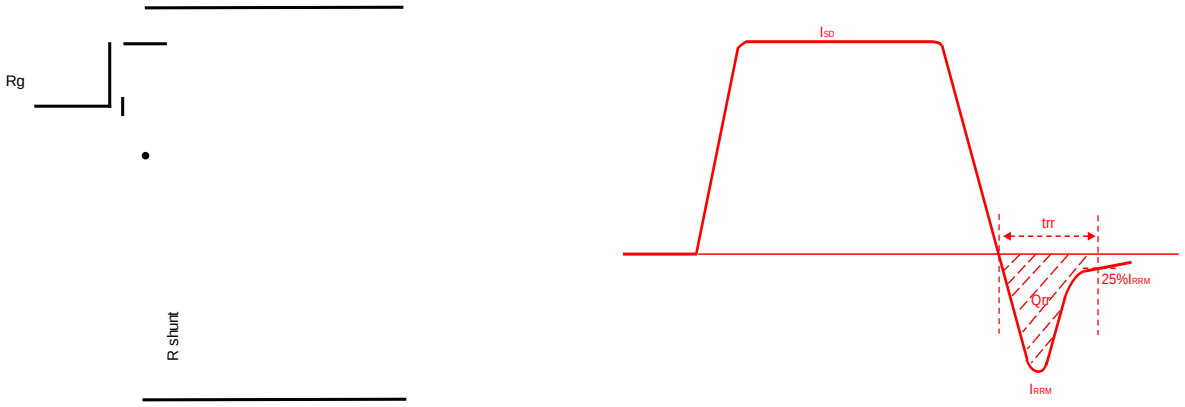
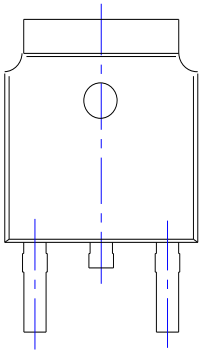


Figure D. Diode Recovery Test Circuit & Waveform

TO-252-B Package information

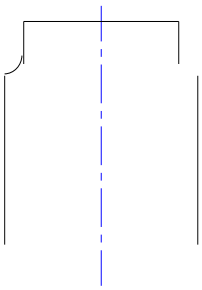


TOP VIEW



SIDE VIEW

DIMENSIONS					
SYMBOL	INCHES				
	MIN.	NOM.			
A1	0.000				
A2	0.087	0.091			
A3	0.035	0.039			
b	0.026	0.030			
c	0.018	0.020			
D	0.256	0.260			
D1					
D2	0.181	0.189			
E	0.390	0.398			
E1	0.236	0.240			



BOTTOM VIEW

SUGGESTED SOLDER PAD LAYOUT

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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