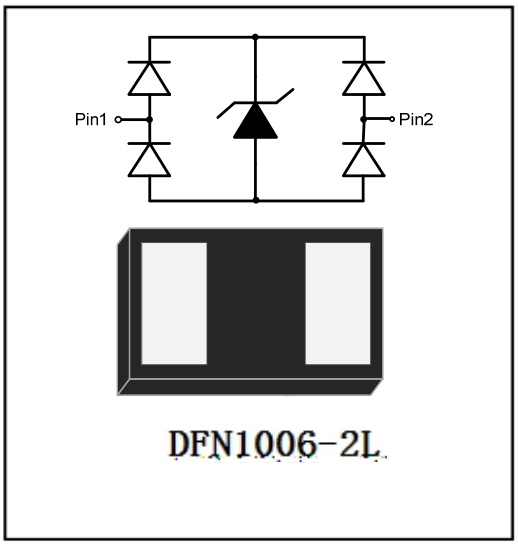
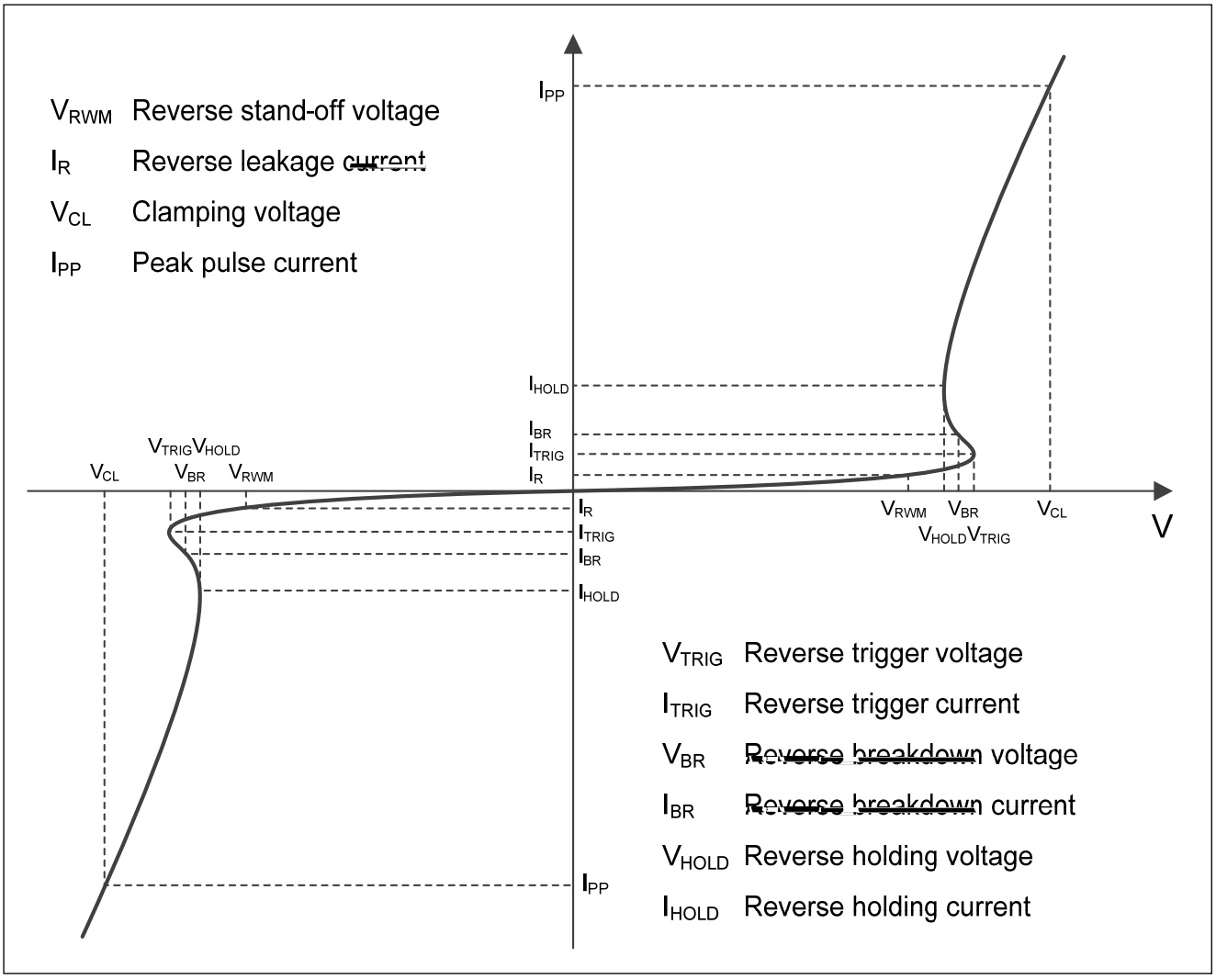


- Stand-off voltage: 5V Max
- Transient protection for each line according to IEC61000-4-2(ESD): ±15kV (contact) IEC61000-4-5(surge): 4A (8/20μs)
- Ultra-low capacitance: C_J = 0.35pF typ
- Ultra-low leakage current: I_R < 1nA typ.
- Low clamping voltage: V_{CL} =14V typ. @ I_{PP} = 16A (TLP)
- Solid-state silicon technology

- : DFN1006-2L
- : Tin plated leads, solderable per J-STD-002 and JESD22-B102
- Cathode line denotes the cathode end
- 5U

■



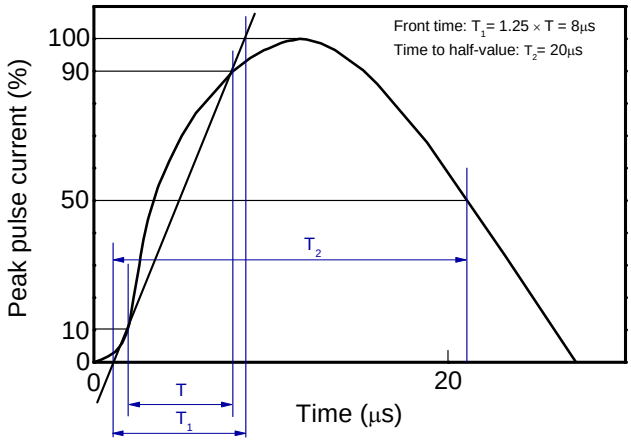
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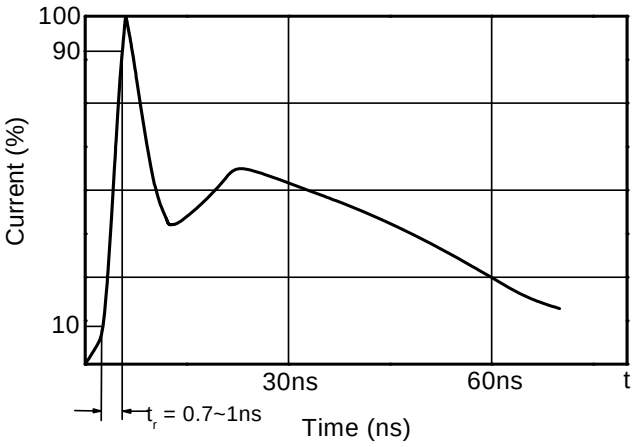
Peak pulse power (t_p = 8/20μs)	P_{pk}	48	W
Peak pulse current (t_p = 8/20μs)	I_{PP}	4	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±15	KV
ESD according to IEC61000-4-2 contact discharge		±15	KV
Junction temperature	T_J	125	°C
Operating temperature	T_{OP}	-40~85	°C
Storage temperature	T_{STG}	-55~150	°C

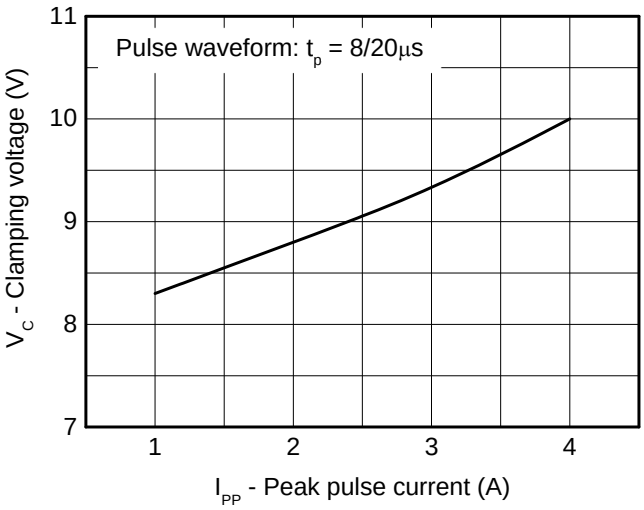
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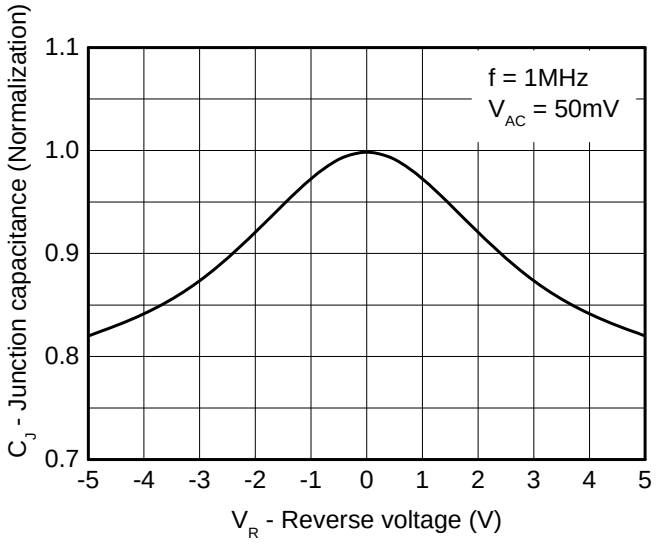
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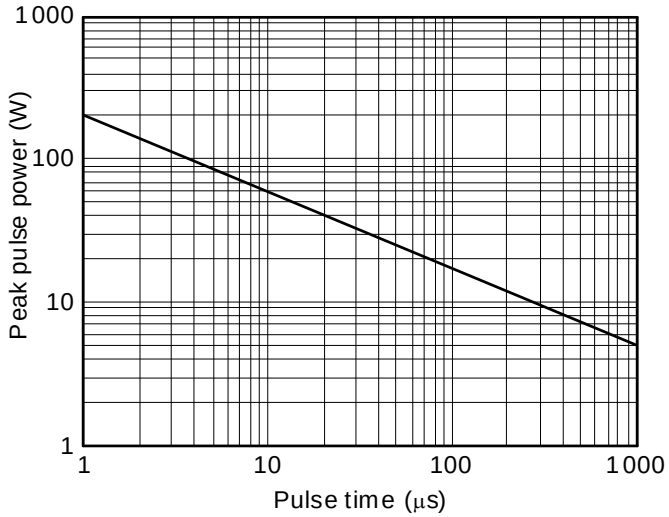
μ

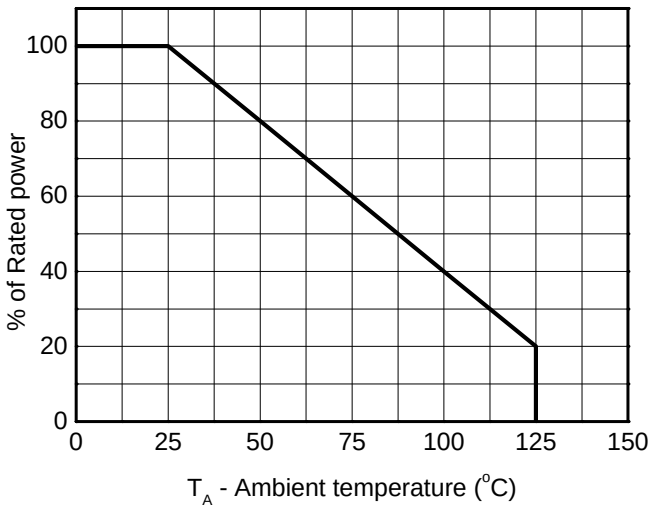

Front time: T_1= 1.25 × T = 8μs
Time to half-value: T_2= 20μs
Peak pulse current (%)
100
90
50
10
0
0
20
T
T_1
T_2
Time (μs)

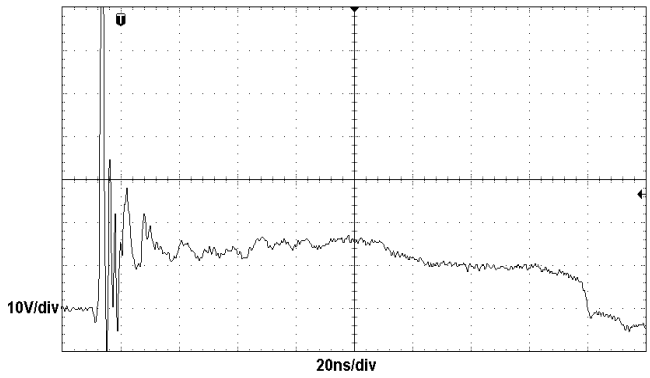

Current (%)
100
90
10
30ns
60ns
t
t_r = 0.7~1ns
Time (ns)

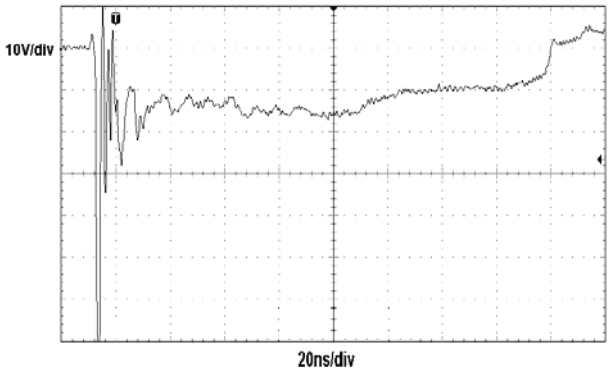

Pulse waveform: t_p = 8/20μs
V_C - Clamping voltage (V)
11
10
9
8
7
1
2
3
4
I_{PP} - Peak pulse current (A)

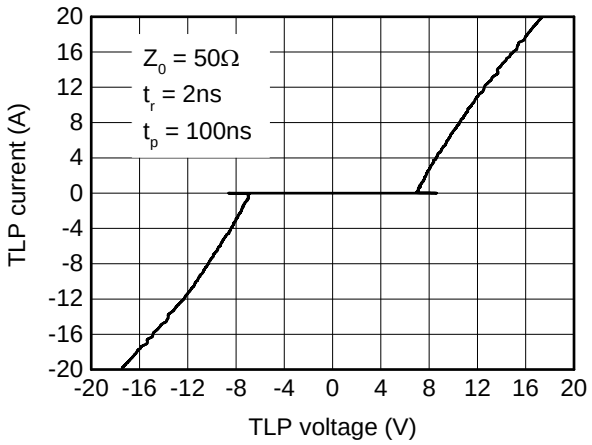

f = 1MHz
V_{AC} = 50mV
C_J - Junction capacitance (Normalization)
1.1
1.0
0.9
0.8
0.7
-5
-4
-3
-2
-1
0
1
2
3
4
5
V_R - Reverse voltage (V)


Peak pulse power (W)
1000
100
10
1
1
10
100
1000
Pulse time (μs)

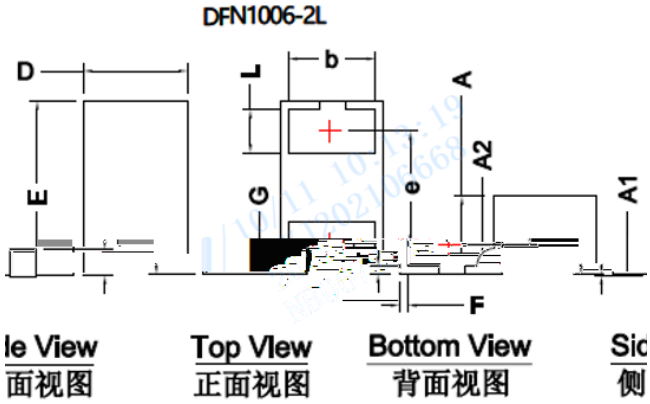

% of Rated power
100
80
60
40
20
0
0
25
50
75
100
125
150
T_A - Ambient temperature (°C)

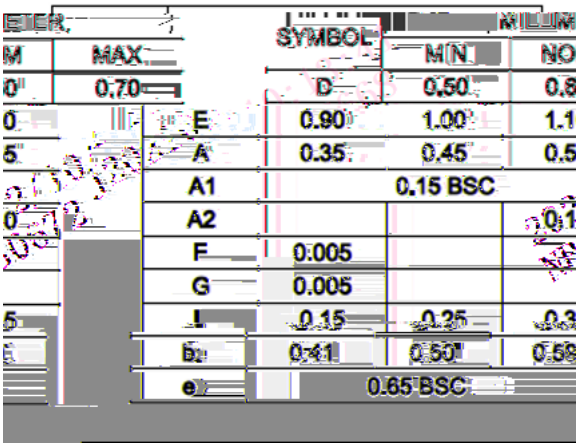

10V/div
20ns/div

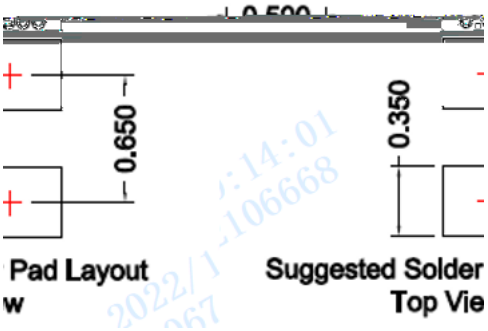

10V/div
20ns/div


Z_0 = 50Ω
t_r = 2ns
t_p = 100ns
TLP current (A)
TLP voltage (V)
20
16
12
8
4
0
-4
-8
-12
-16
-20
-20 -16 -12 -8 -4 0 4 8 12 16 20

■


DFN1006-2L
D
E
L
b
G
e
A
A2
A1
F
le View
面视图
Top View
正面视图
Bottom View
背面视图
Sic
侧


SYMBOL
MIN
MAX
D
0.50
0.70
E
0.90
1.00
A
0.35
0.45
A1
0.15 BSC
A2
F
0.005
G
0.005
b
0.41
0.50
e
0.65 BSC



Note:
1.Controlling dimension:In millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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