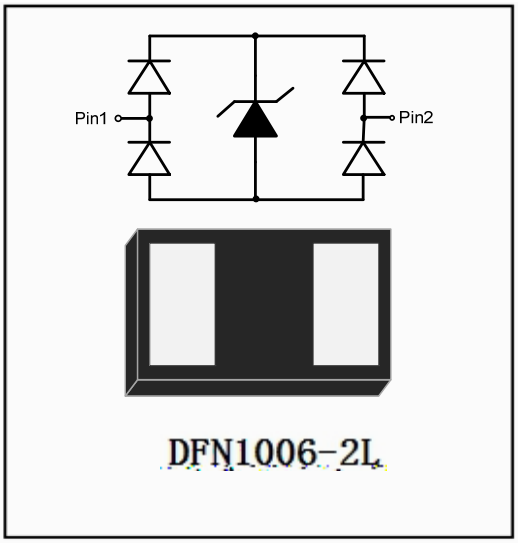
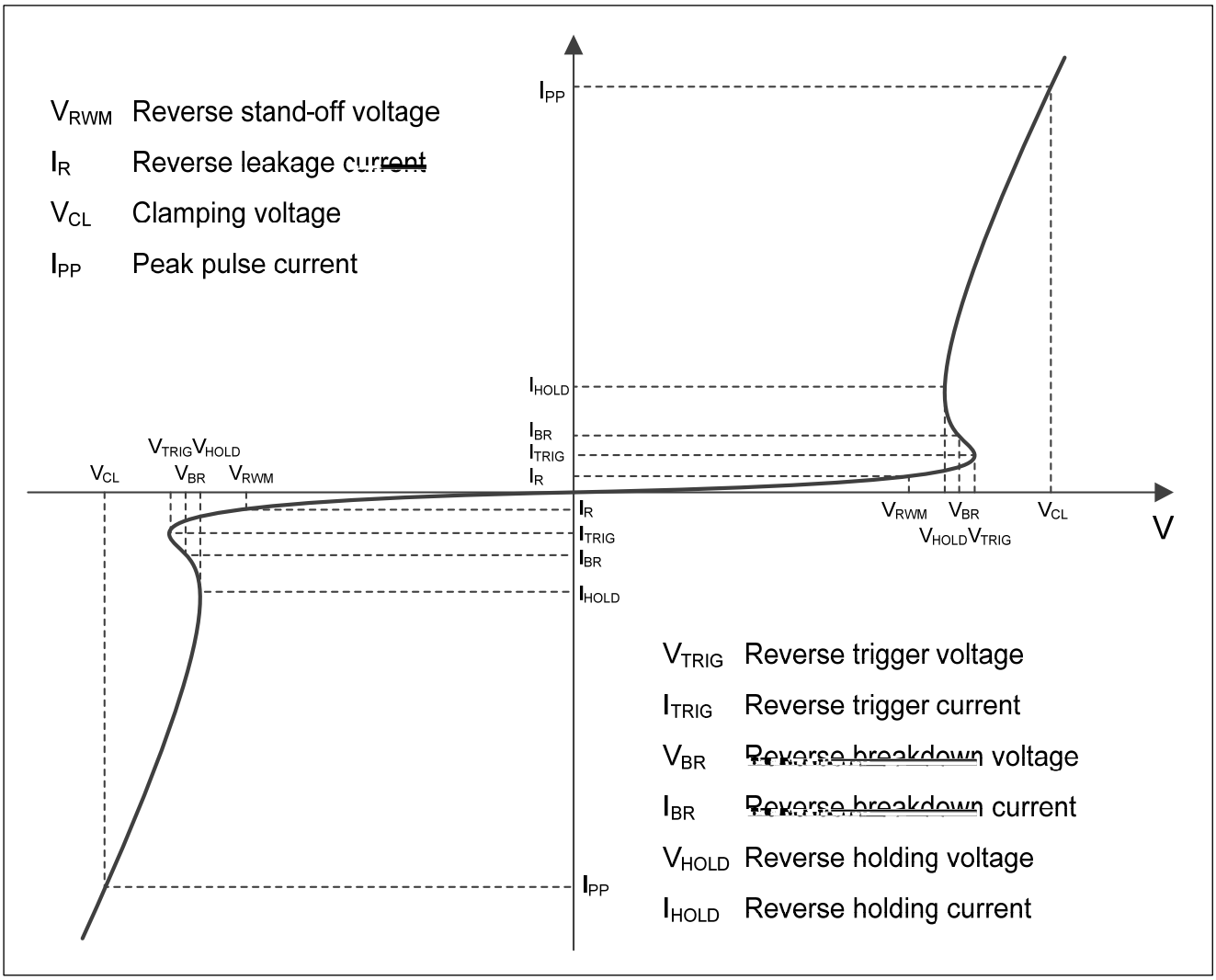


- Stand-off voltage: ±5V Max
- Transient protection for each line according to
IEC61000-4-2(ESD): ±30kV (contact)
IEC61000-4-4 (EFT): 40A (5/50ns)
IEC61000-4-5(surge): 15A (8/20μs)
- Ultra-low capacitance: C_J = 1.35pF typ
- Ultra-low leakage current: I_R < 1nA typ.
- Low clamping voltage: V_{CL} =12V typ. @ I_{PP} = 16A (TLP)
- Solid-state silicon technology

- : DFN1006-2L
- : Tin plated leads, solderable per J-STD-002 and JESD22-B102
- Cathode line denotes the cathode end
- 5S

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Peak pulse power (t_p = 8/20μs)	P_{pk}	210	W
Peak pulse current (t_p = 8/20μs)	I_{PP}	15	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±30	KV
ESD according to IEC61000-4-2 contact discharge		±30	KV
Junction temperature	T_J	125	°C
Operating temperature	T_{OP}	-40~85	°C
Storage temperature	T_{STG}	-55~150	°C

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Reverse maximum working voltage	V_{RWM}	V				±5
Reverse leakage current	I_R	nA	V_{RWM} =5V		<1	50
Reverse breakdown voltage	V_{BR}	V	I_{BR} = 1mA	6	8	
Reverse holding voltage	V_{HOLD}	V	I_{HOLD} = 500mA	5	7	
Clamping voltage [1)]	V_{CL}	V	I_{PP} = 16A, t_p = 100ns		12	
Dynamic resistance [1)]	R_{DYN}	Ω			0.3	
Clamping voltage [2)]	V_{CL}	V	V_{ESD} = 8kV		12	
Clamping voltage [3)]	V_{CL}	V	I_{PP} = 1A, t_p = 8/20μs		8	10
		V	I_{PP} = 15A,t_p = 8/20μs		12	14
Junction capacitance	C_J	pF	V_R = 0V, f = 1MHz		1.35	1.55

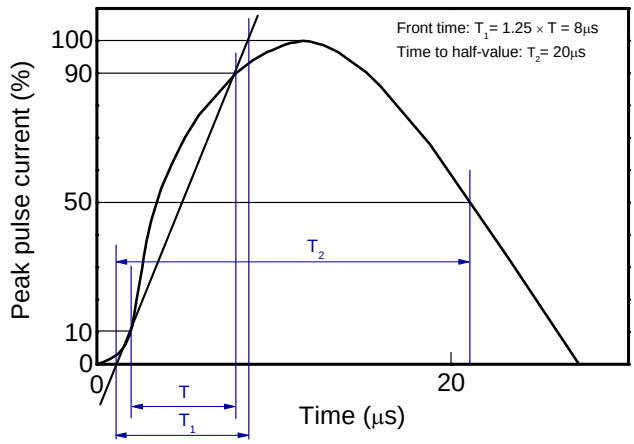
(1). TLP parameter: Z_0 = 50Ω, t_p = 100ns, t_r = 2ns, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.
(2). Contact discharge mode, according to IEC61000-4-2.
(3). Non-repetitive current pulse, according to IEC61000-4-5.

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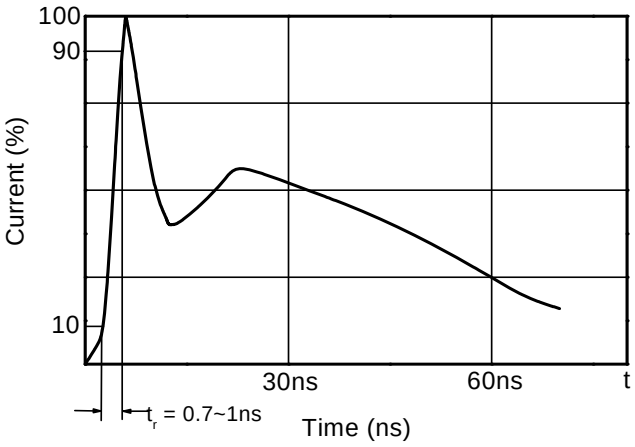
ESDSLC5V0LBA	Approximate 0.9	10000	100000	400000	Tape& reel

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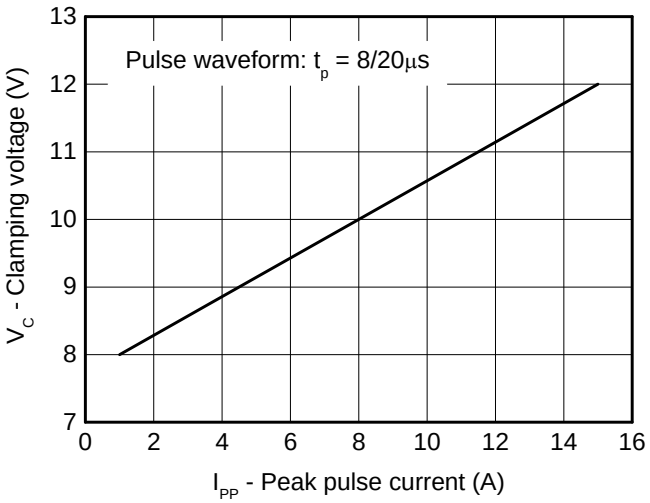
8/20μs waveform per IEC61000-4-5



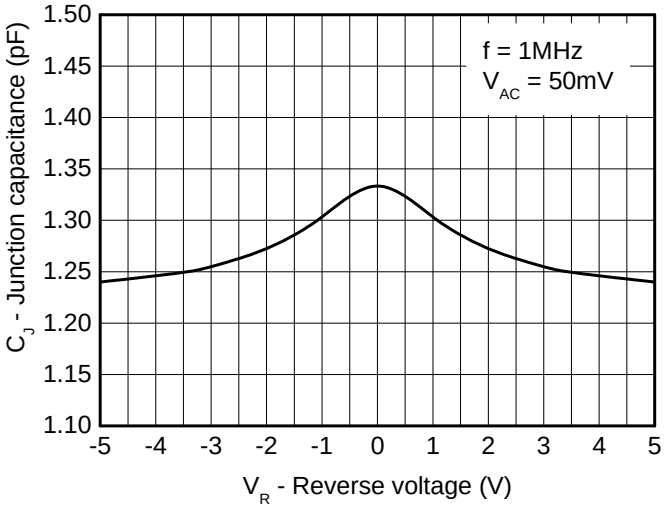
Contact discharge current waveform per IEC61000-4-2



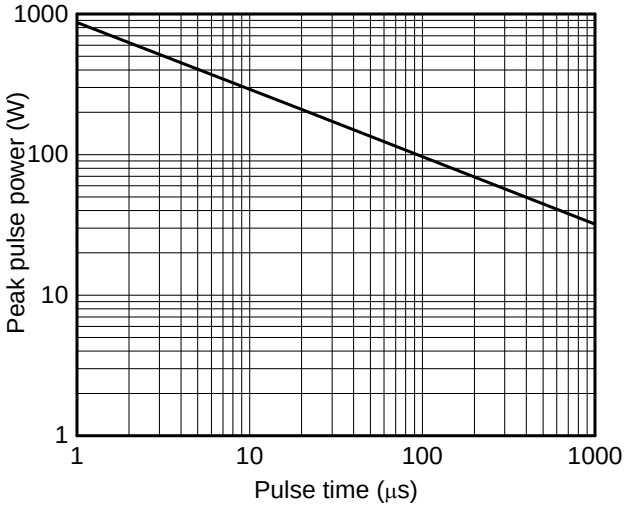
Clamping voltage vs. Peak pulse current



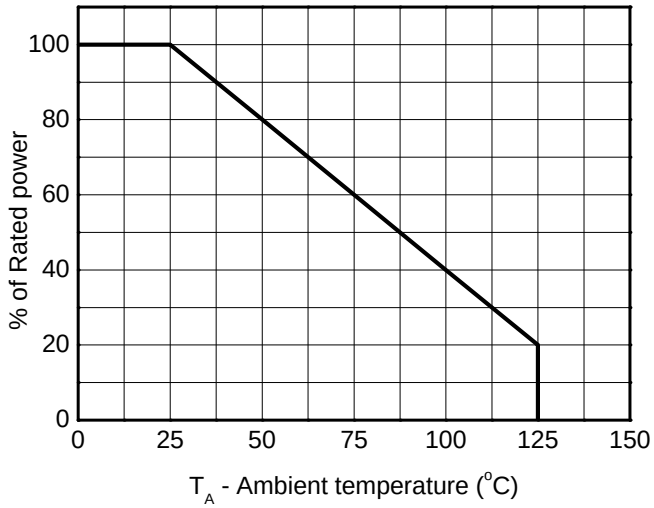
Capacitance vs. Reverse voltage



Non-repetitive peak pulse power vs. Pulse time



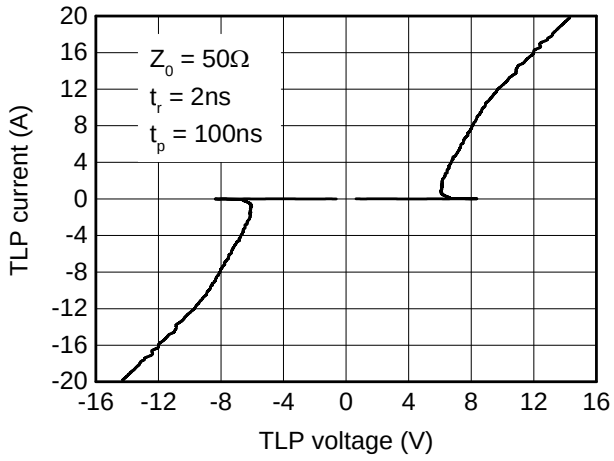
Power derating vs. Ambient temperature



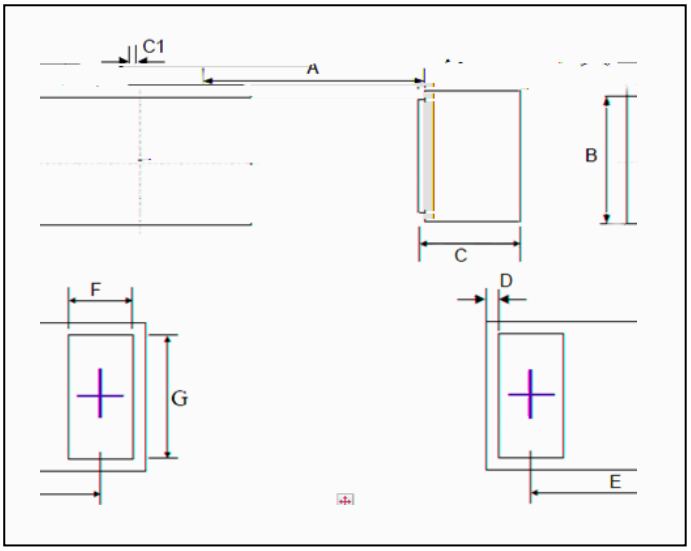
ESD clamping
(+8kV contact discharge per IEC61000-4-2)

ESD clamping
(-8kV contact discharge per IEC61000-4-2)

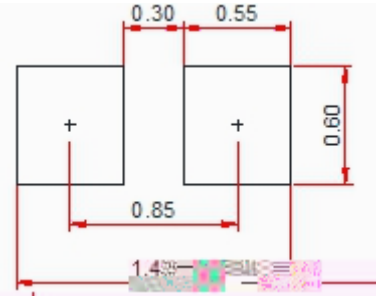
TLP Measurement



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Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met