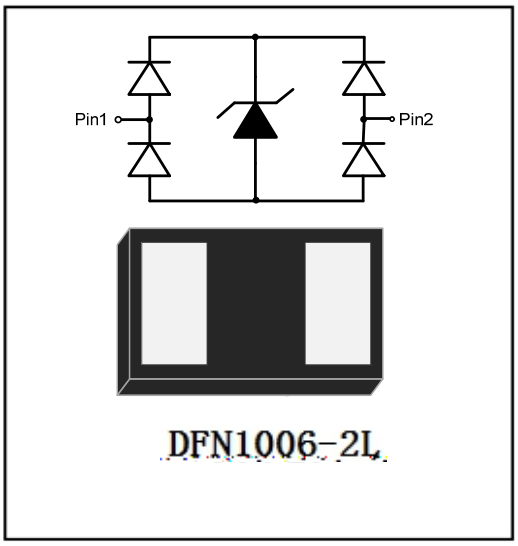
1- Line, Bi-directional, Ultra-low Capacitance Transient Voltage Suppressor

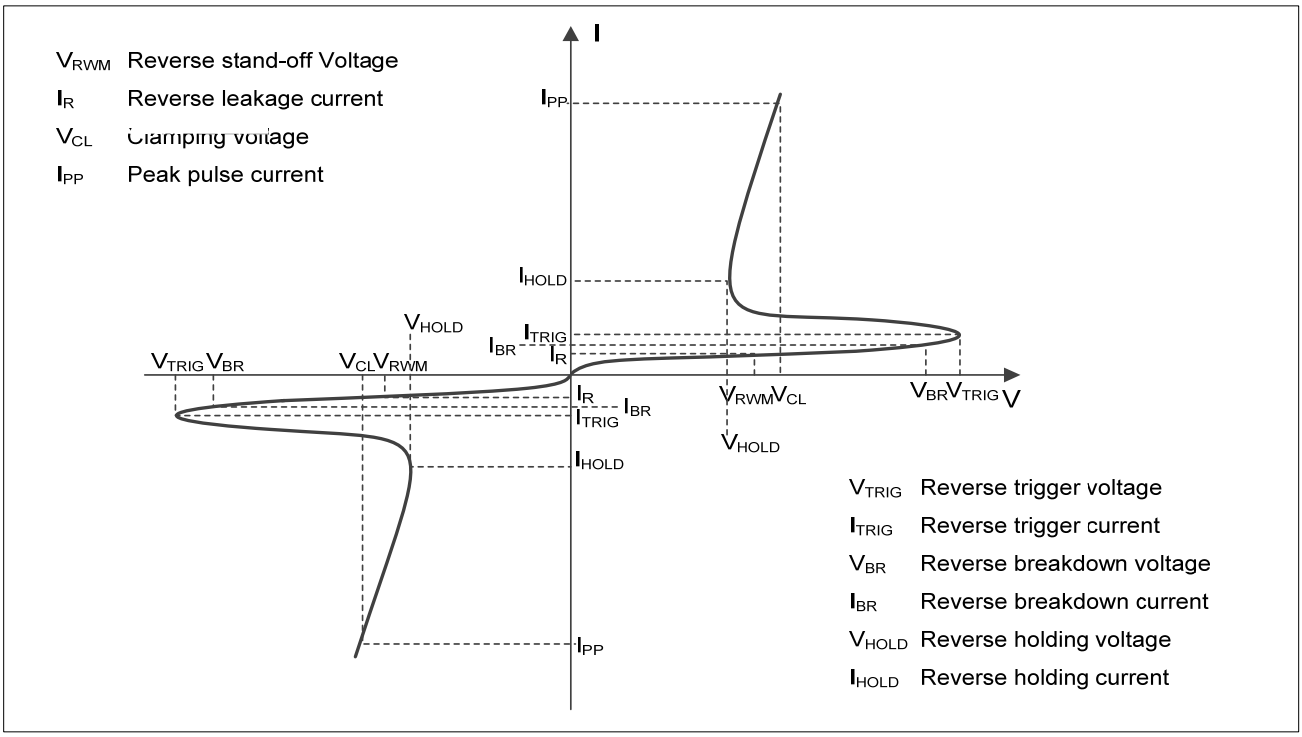


Features

- Stand-off voltage: 3.3V Max
- Transient protection for each line according to IEC61000-4-2(ESD): ±15kV (contact) IEC61000-4-5(surge): 8A (8/20μs)
- Ultra-low capacitance: C_J = 0.8pF typ
- Ultra-low leakage current: I_R < 1nA typ.
- Low clamping voltage: V_{CL} = 6.3V typ. @ I_{PP} = 16A (TLP)
- Solid-state silicon technology

Mechanical Data

- **Package**: DFN1006-2L
- **Terminals**: Tin plated leads, solderable per J-STD-002 and JESD22-B102



■Maximum Ratings

PARAMETER	SYMBOL	Rating	UNIT
Peak pulse power (t_p = 8/20μs)	P_{pk}	68	W
Peak pulse current (t_p = 8/20μs)	I_{PP}	7	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±30	KV
ESD according to IEC61000-4-2 contact discharge		±30	KV
Junction temperature	T_J	125	°C
Operating temperature	T_{OP}	-40~85	°C
Storage temperature	T_{STG}	-55~150	°C

■Electrical Characteristics T_a=25 Unless otherwise specified

PARAMETER	Symbol	UNIT	Conditions	Min	Typ	Max
Reverse maximum working voltage	V_{RWM}	V				3.3
Reverse leakage current	I_R	nA	V_{RWM} =3.3V			50
Reverse breakdown voltage	V_{BR}	V	I_{BR} = 1mA	7.0	10.0	
Clamping voltage 1)	V_{CL}	V	I_{PP} = 16A, t_p = 100ns		6.3	
Dynamic resistance 1)	R_{DYN}	Ω			0.17	
Clamping voltage 2)	V_{CL}	V	V_{ESD} = 8kV		6.3	
Clamping voltage 3)	V_{CL}	V	I_{PP} = 1A, t_p = 8/20μs		3.2	4.5
		V	I_{PP} = 7A,t_p = 8/20μs		6.5	8.5
Junction capacitance	C_J	pF	V_R = 0V, f = 1MHz		0.8	1

(1). TLP parameter: Z_0 = 50Ω, t_p = 100ns, t_r = 2ns, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

(2). Contact discharge mode, according to IEC61000-4-2.

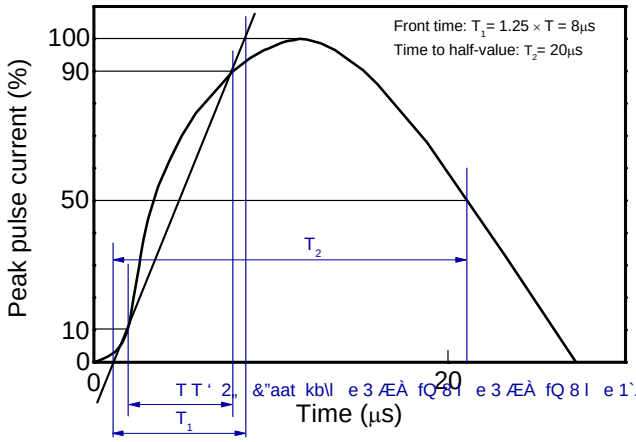
(3). Non-repetitive current pulse, according to IEC61000-4-5.

■Ordering Information (Example)

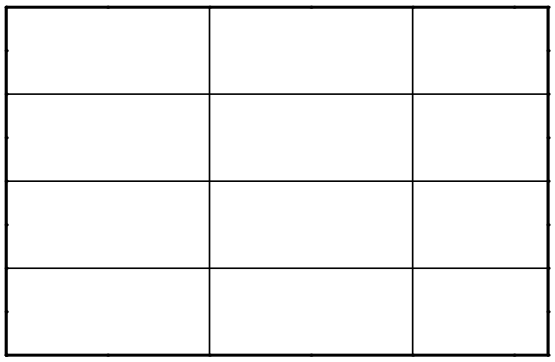
PREFERED P/N	UNIT WEIGHT(mg)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
ESDSLC3V3LBA	Approximate 0.9	10000	100000	400000	Tape&reel

■ Characteristics (Typical)

8/20 s waveform per IEC61000-4-5



Contact discharge current waveform per IEC61000-4-2



T T ‘ 2, &”aat kb\l e 3 ÆÀ fQ 8 l e 3 ÆÀ fQ 8 l e 1`ÆÀ fQ 8 l e 3 ÆÀ fQ l e 3€ÆÀ fQ 2 l e 3€ÆÀ fQ 2 l e&(.Q0V&(. 0 !, HQ0V À … a!, 1 À .

Clamping voltage vs. Peak pulse current

Capacitance vs. Reverse voltage

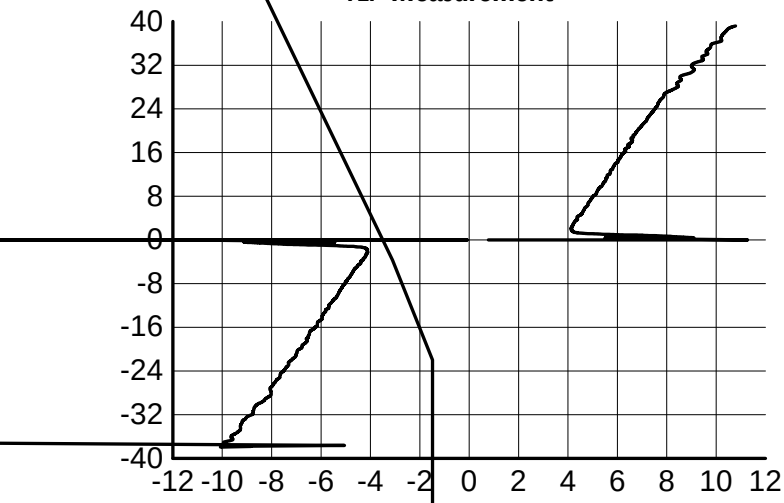
Non-repetitive peak pulse power vs. Pulse time

Power derating vs. Ambient temperature

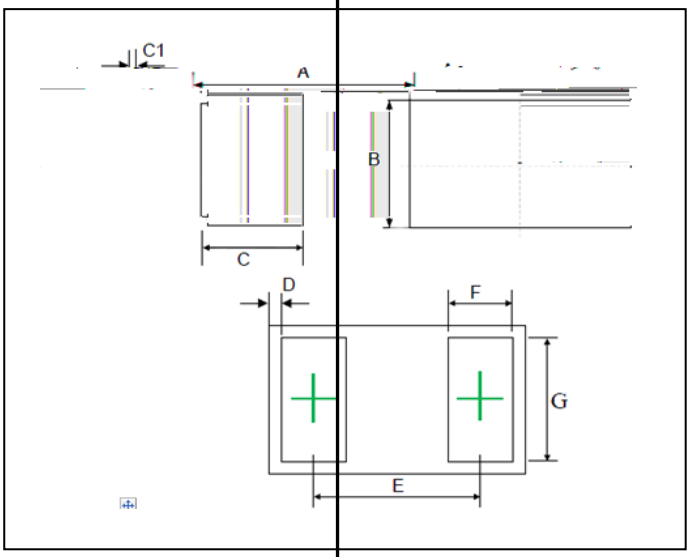
ESD clamping
(+8kV contact discharge per IEC61000-4-2)

ESD clamping
(-8kV contact discharge per IEC61000-4-2)

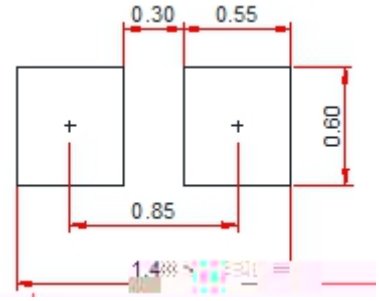
TLP Measurement



■ Outline Dimensions



■ **Recommend land pattern** (Unit:mm)



Notes:
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met

Disclaimer

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